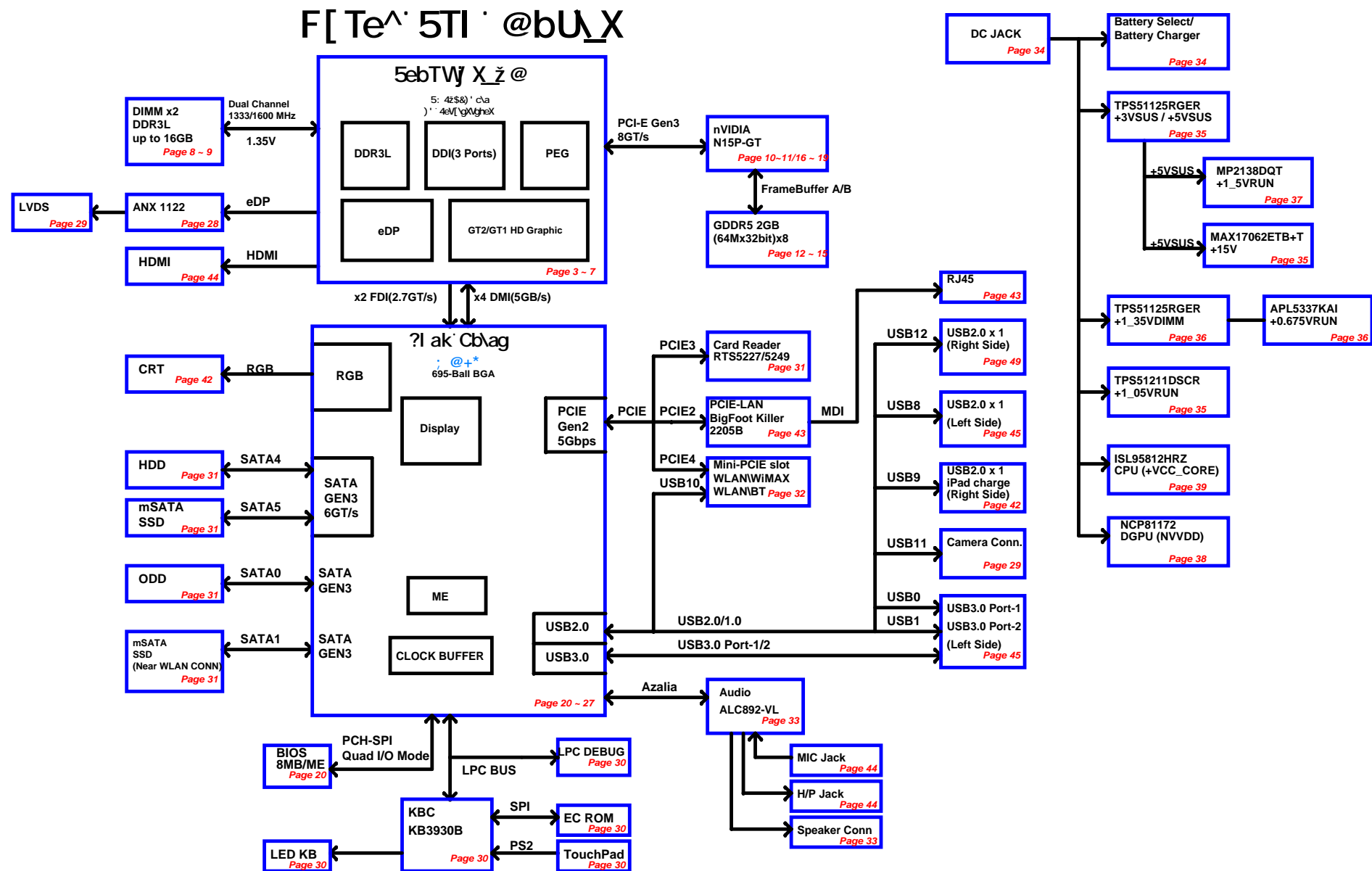


MS-16GH ver:0A

F[Te^ 5TI · @bU_X



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

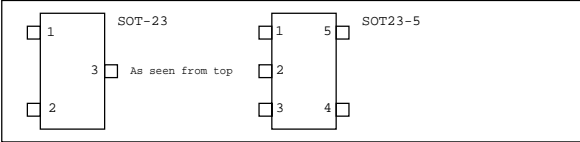
Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	PM_SLP_S4#
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	PM_SLP_S3#
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	PM_SLP_S3#
+1_5VRUN	1.5V switched power rail (off in S3-S5)	PM_SLP_S3#
+VCC_CORE	1.8V Core Voltage for Processor	VR_ON
+1_05VRUN	1.05V rail for Processor	PM_SLP_S3#
NVVD	0.6~1.2V(VBoot:0.9V)Core Voltage for nVIDIA N14E-GE DGPU	GPIO11_GPUVID
+3V3_NV	3.3V GPU I/O power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	GPU_PWRGD
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	GPU_PWRGD

Net Naming Conventions

Suffix
= Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

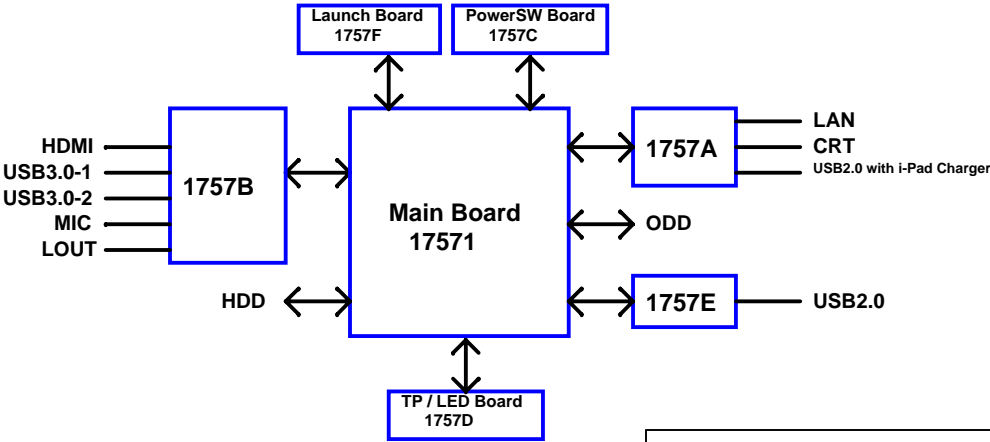
PCB Footprints

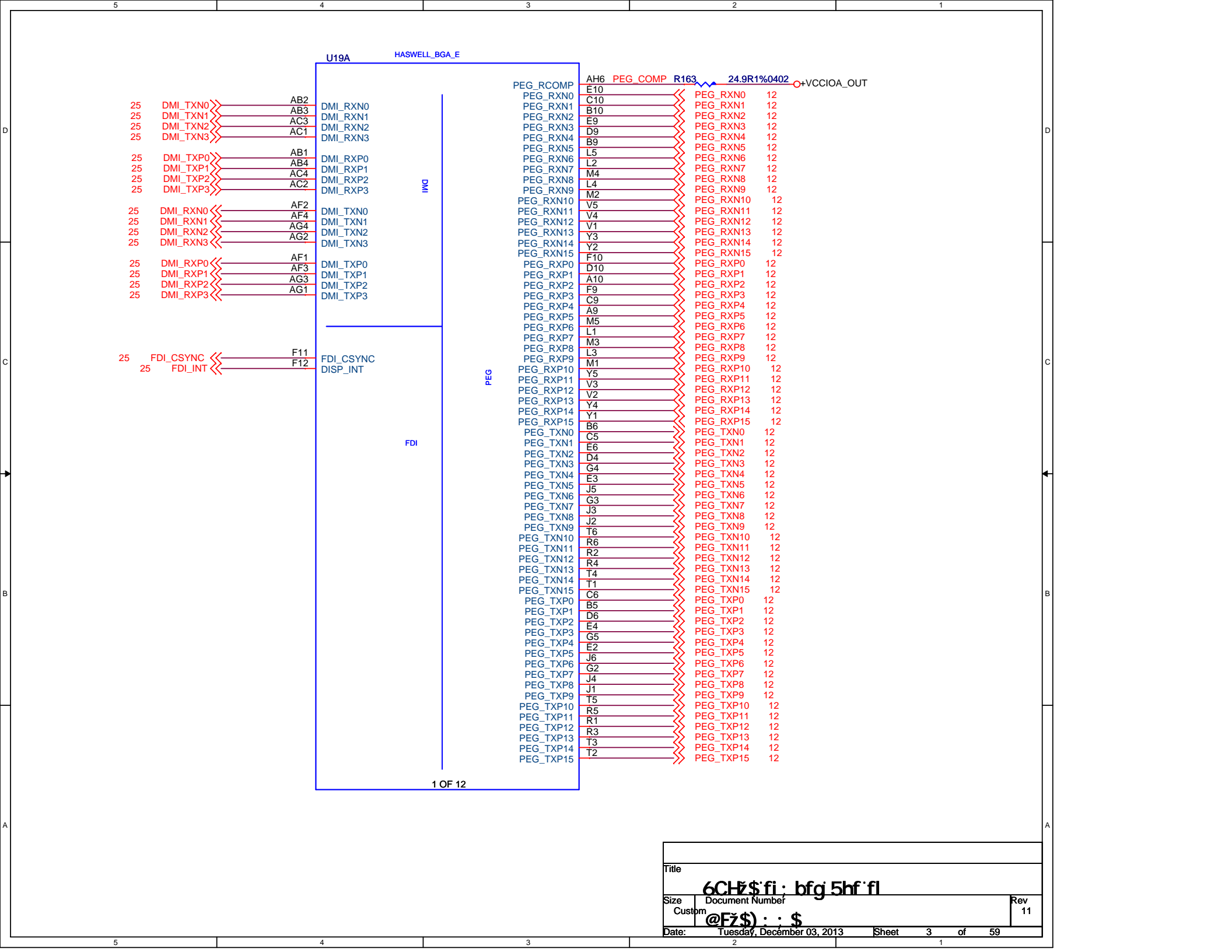


POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

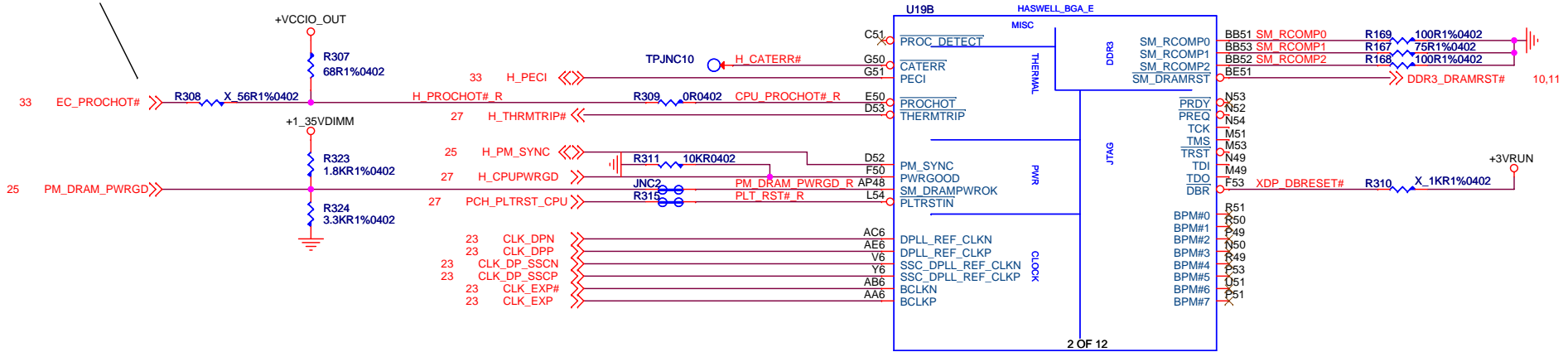
Note : WHEN AC MODE , System turn on then +V*SUS will always keep high



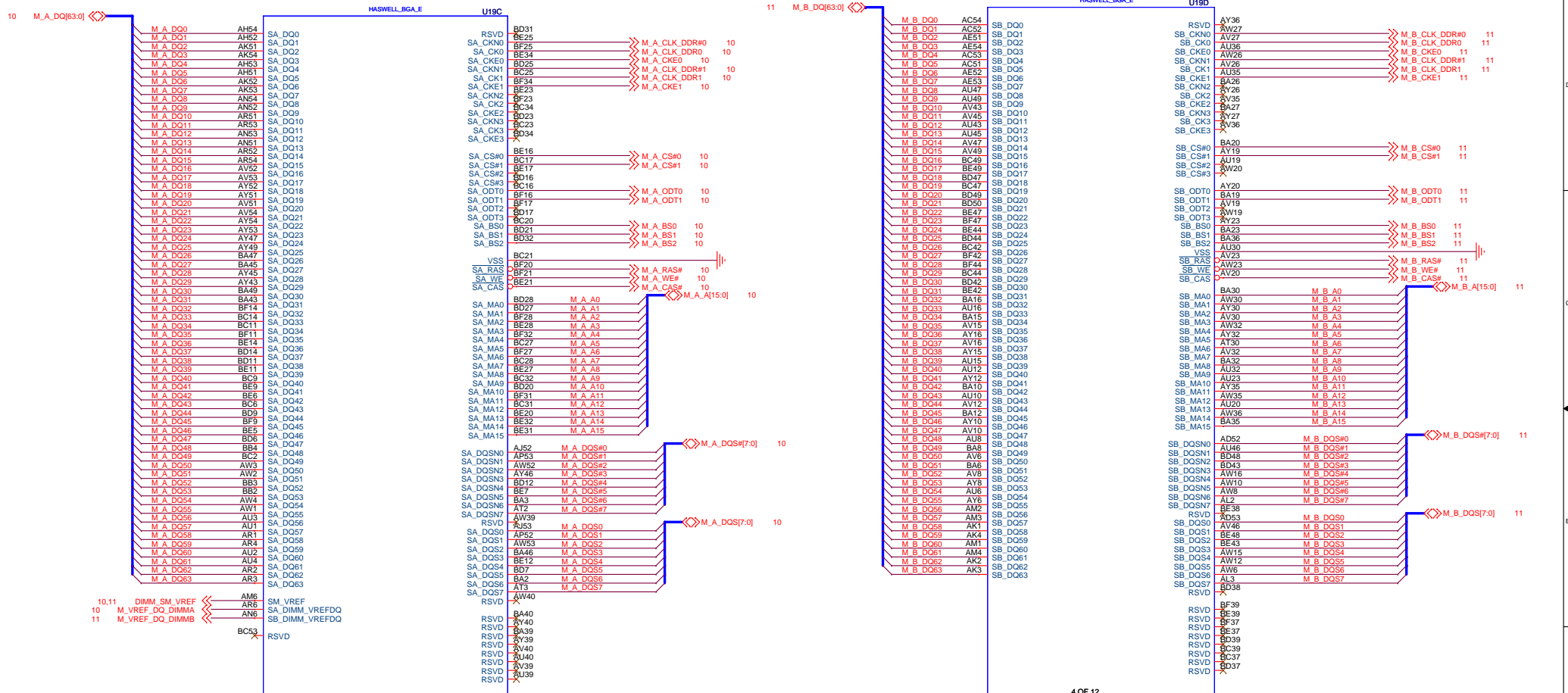


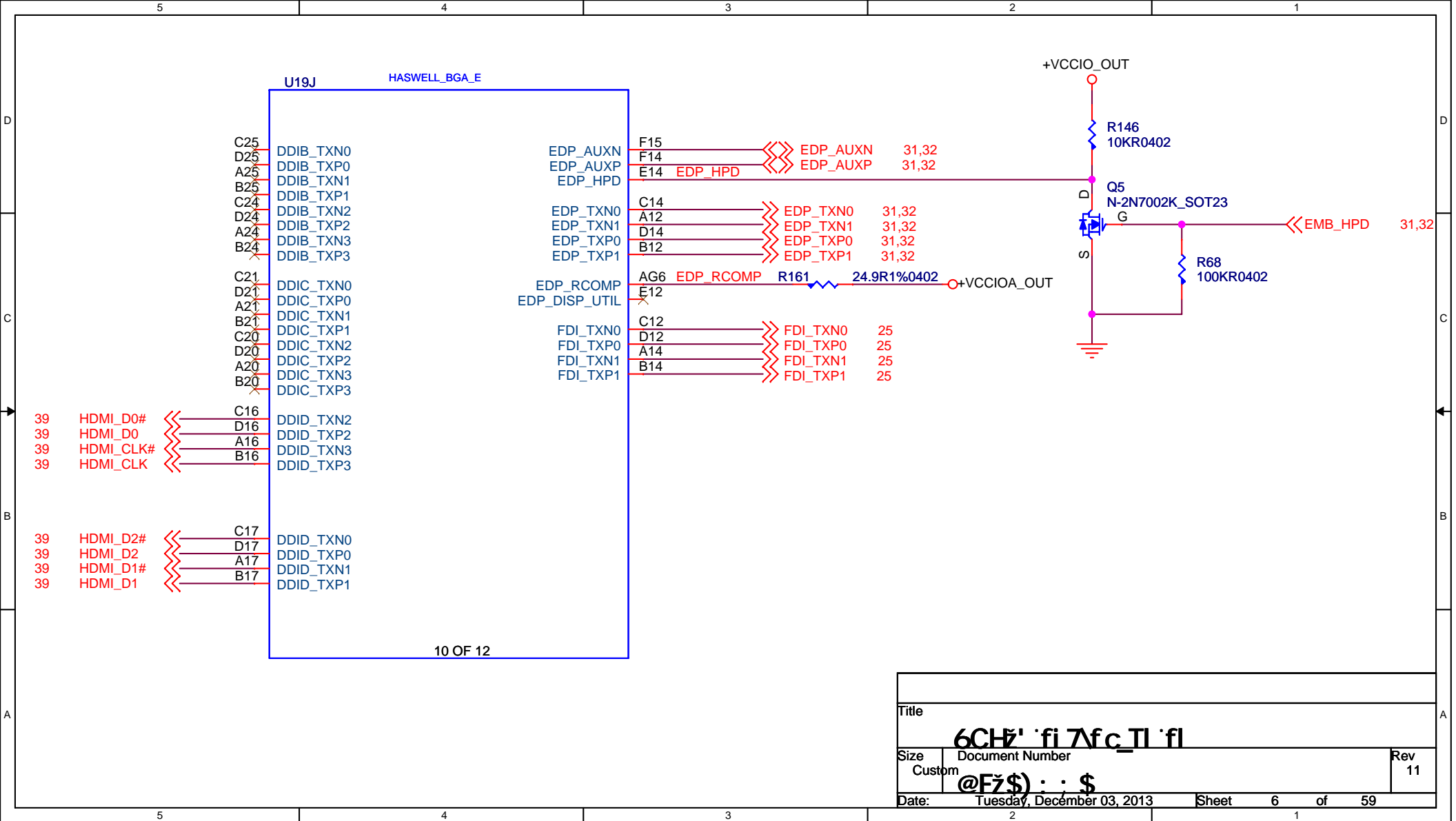
Title		
6CH\$'fi : bfg 5hf'fl		
Size	Document Number	Rev
Custom	@Fz\$) : . \$	11
Date:	Tuesday, December 03, 2013	Sheet 3 of 59

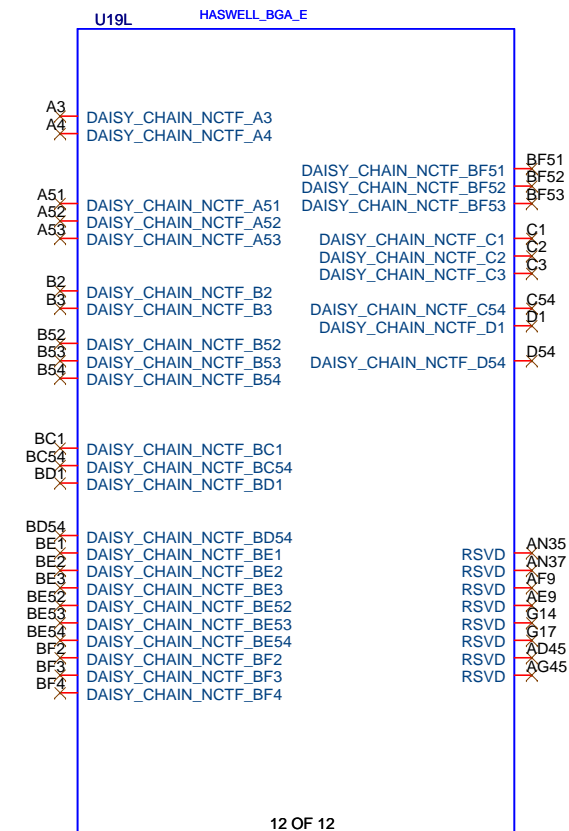
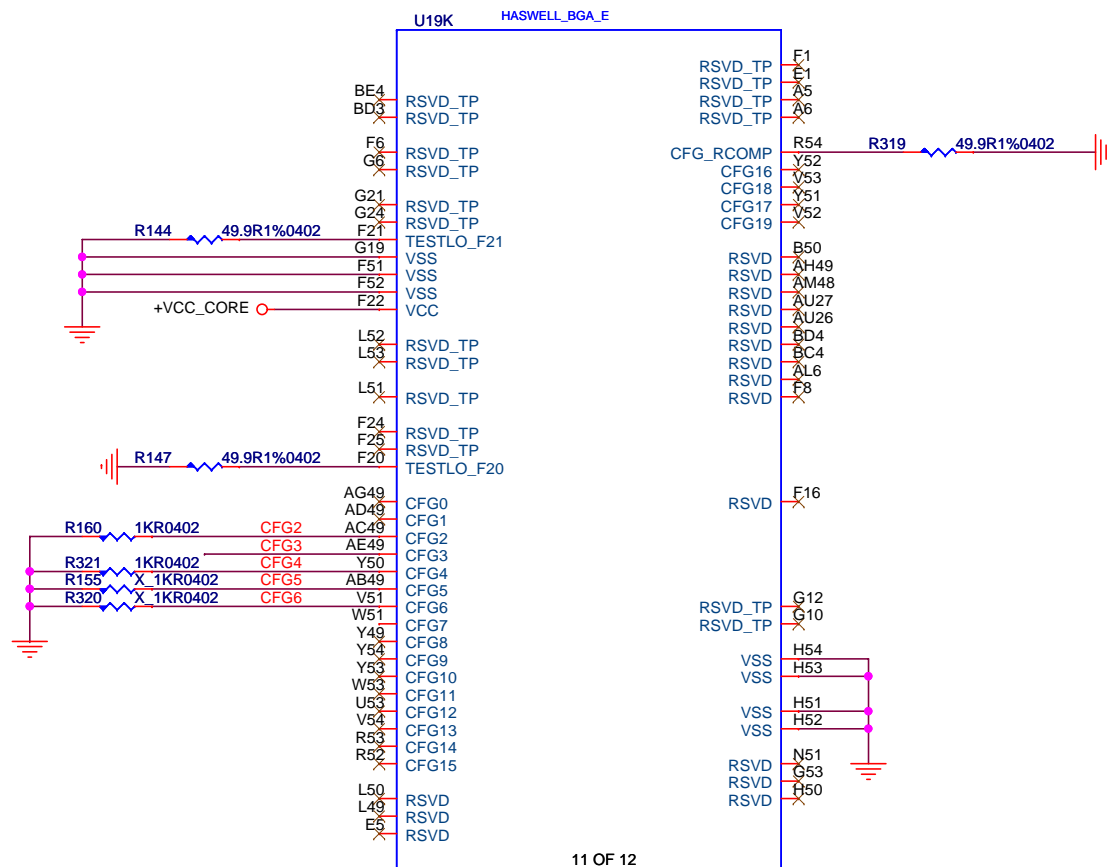
[Fuqun] 1.0V in CPU, EC set OD output



Title			
6CH?%fi 6?>" @F6 fl			
Size	Document Number		Rev
Custom	@F7\$) : : \$		11
Date:	Tuesday, December 03, 2013	Sheet	4 of 59







PCI Express® Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP enable	
CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

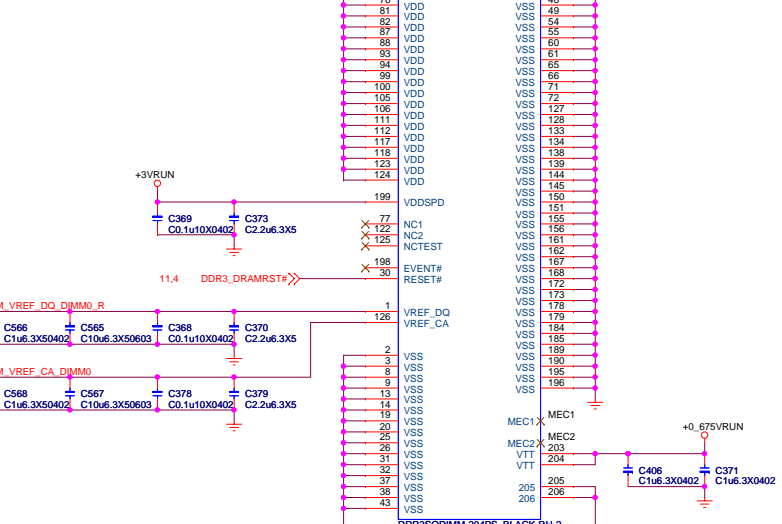
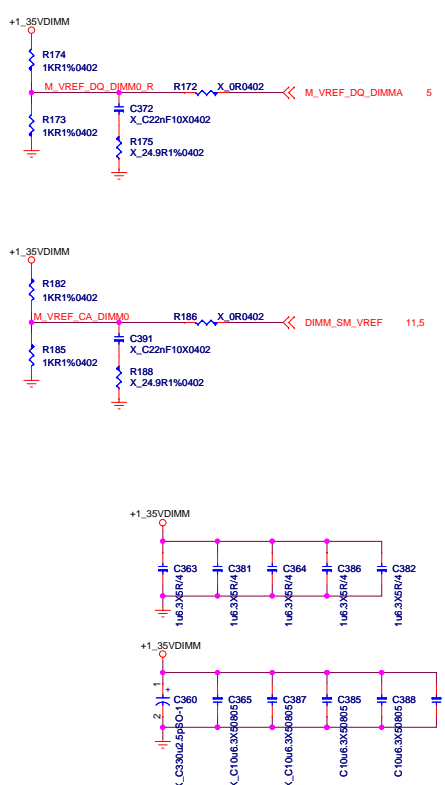
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Title				
6CHZ('fi 69: "EXFxi XWFI				
Size	Document Number			Rev
Custom	@F7\$) : : \$			11
Date:	Tuesday, December 03, 2013	Sheet	7	of 59

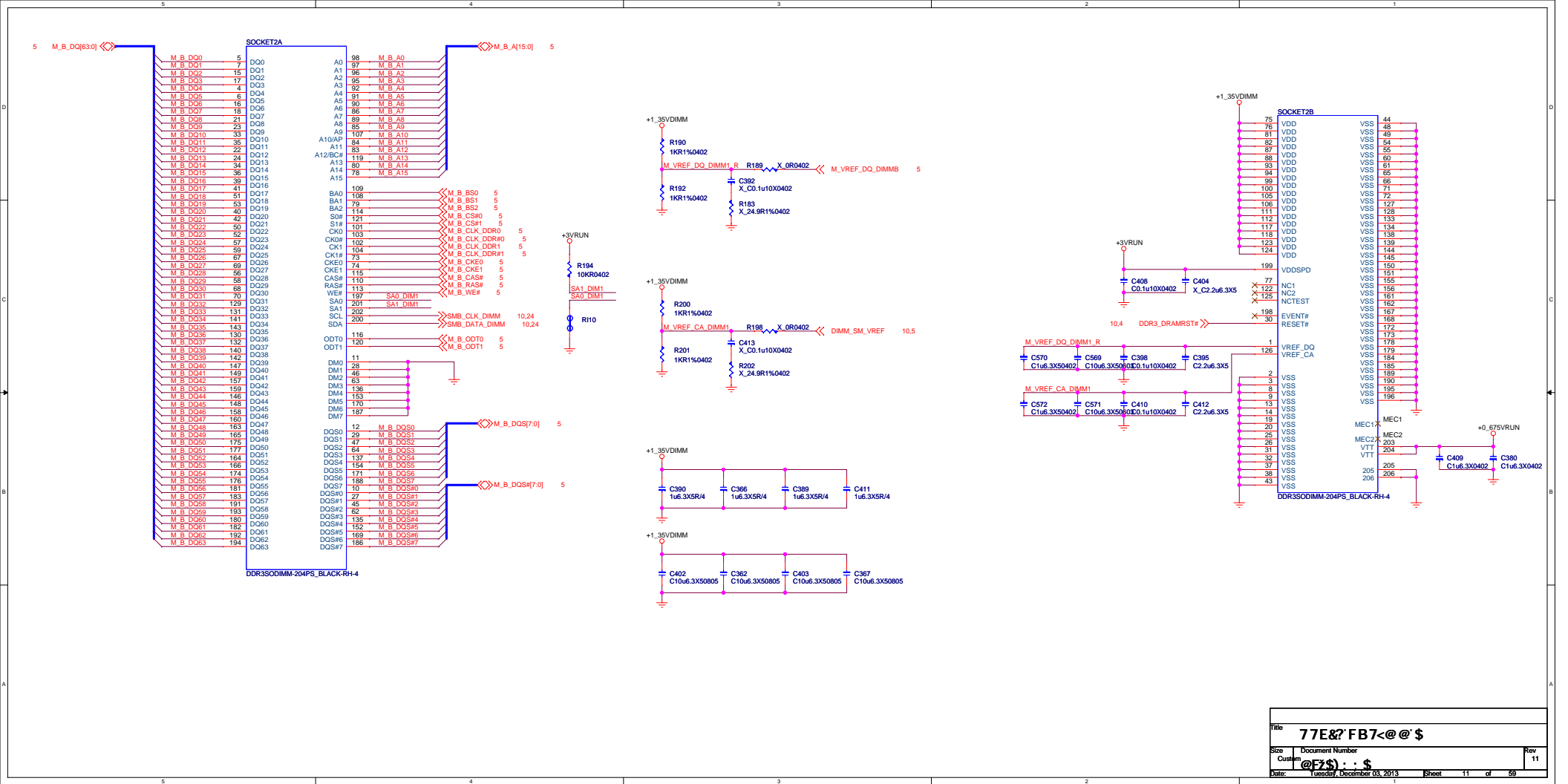




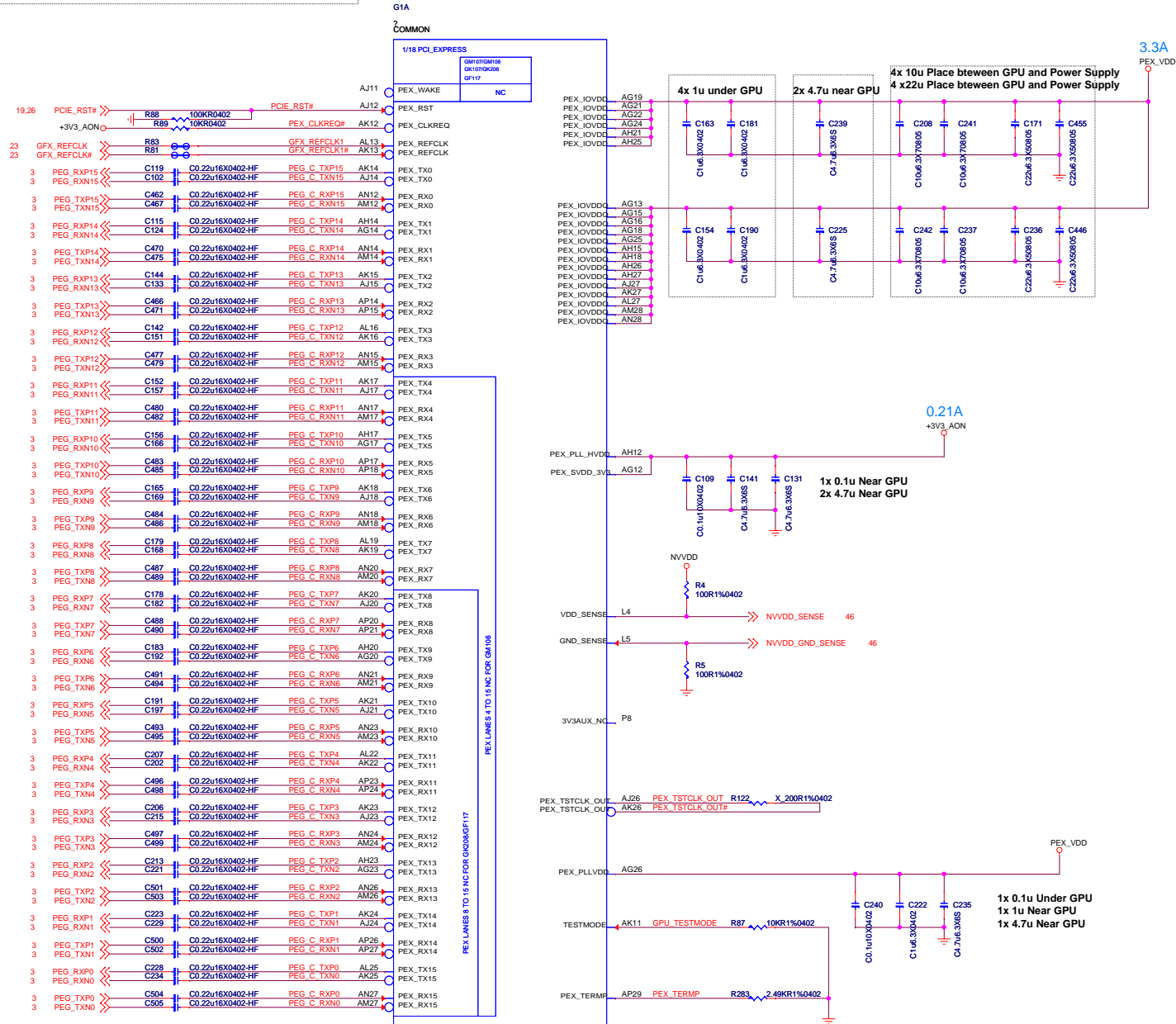
DDR3SODIMM-204PS_BLACK-RH-2



Title	
77E&?FB7<@#@#	
Size	Document Number
Custom	@F\$)
Date:	Tuesday, December 03, 2013
Sheet	10 of 59

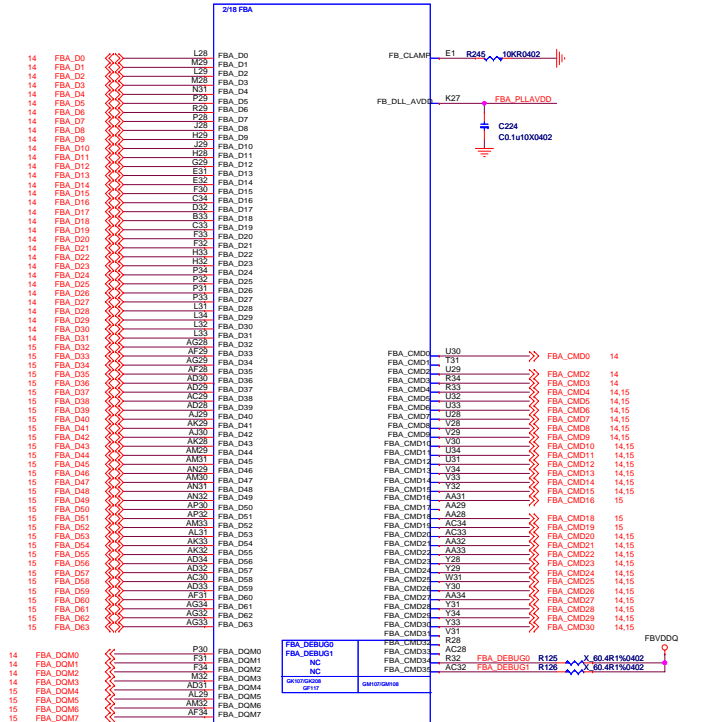


G1A

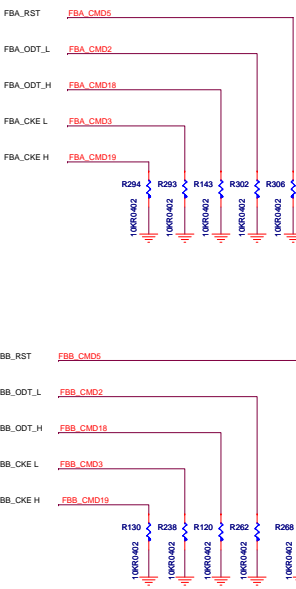


G1B

COMMON

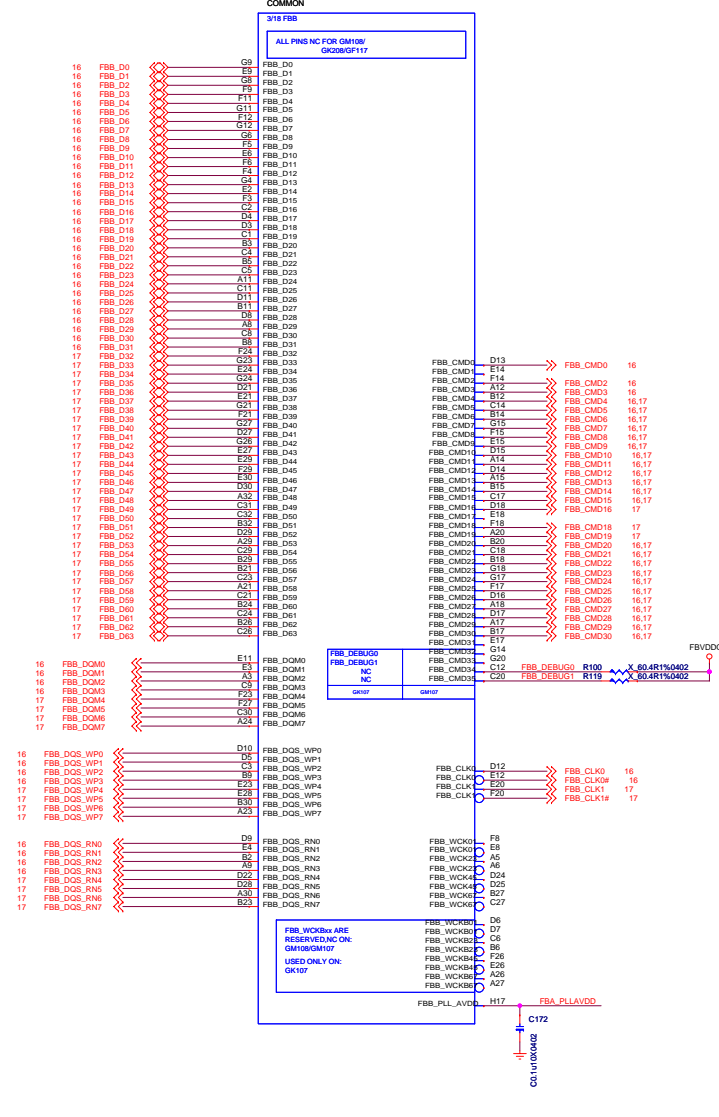


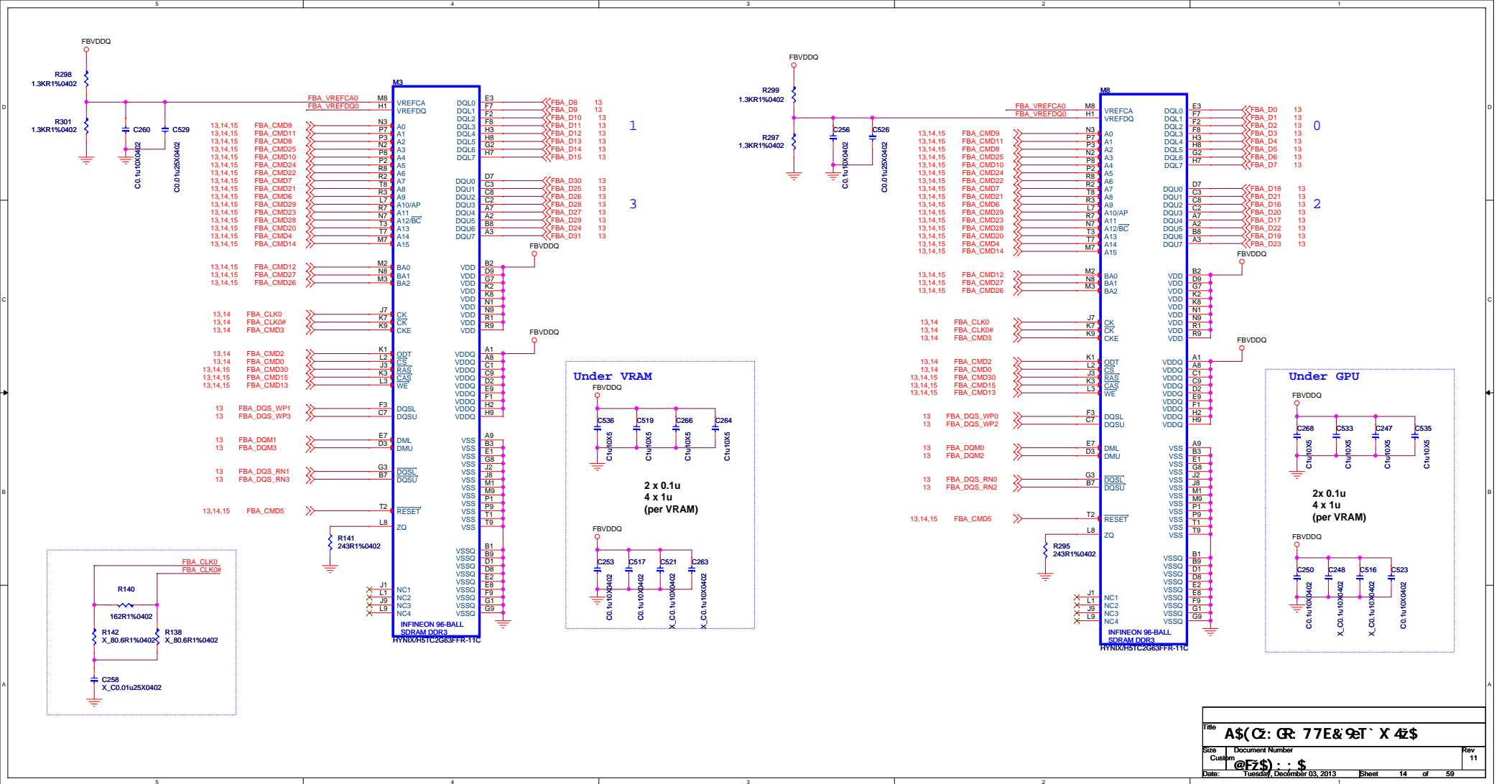
	Data[0-31]	Data[32-63]
PEX_CMD0	CS0	
PEX_CMD1		
PEX_CMD2	ODT	
PEX_CMD3	CKE	
PEX_CMD4	A14	A14
PEX_CMD5	RST	RST
PEX_CMD6	A9	A9
PEX_CMD7	A7	A7
PEX_CMD8	A2	A2
PEX_CMD9	A0	A0
PEX_CMD10	A4	A4
PEX_CMD11	A1	A1
PEX_CMD12	BA0	BA0
PEX_CMD13	WE	WE
PEX_CMD14	A15	A15
PEX_CMD15	CAS	CAS
PEX_CMD16	CS0	
PEX_CMD17		
PEX_CMD18	ODT	
PEX_CMD19	CKE	
PEX_CMD20	A13	A13
PEX_CMD21	A8	A8
PEX_CMD22	A6	A6
PEX_CMD23	A11	A11
PEX_CMD24	A5	A5
PEX_CMD25	A3	A3
PEX_CMD26	BA2	BA2
PEX_CMD27	BA1	BA1
PEX_CMD28	A12	A12
PEX_CMD29	A10	A10
PEX_CMD30	RAS	RAS
PEX_CMD31		
PEX_CMD32		
PEX_CMD33		
PEX_CMD34	DBQ0	
PEX_CMD35	DBQ1	

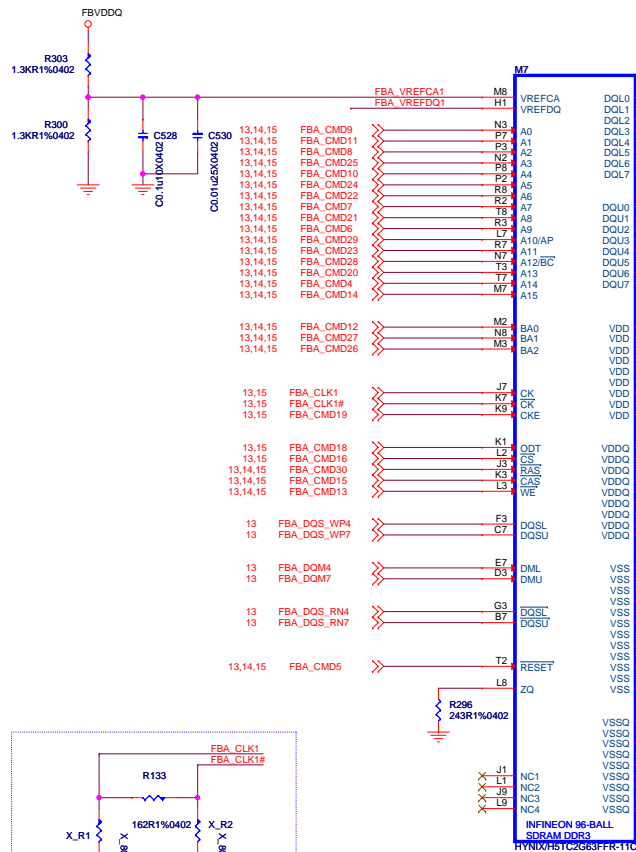


G1C

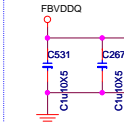
COMMON



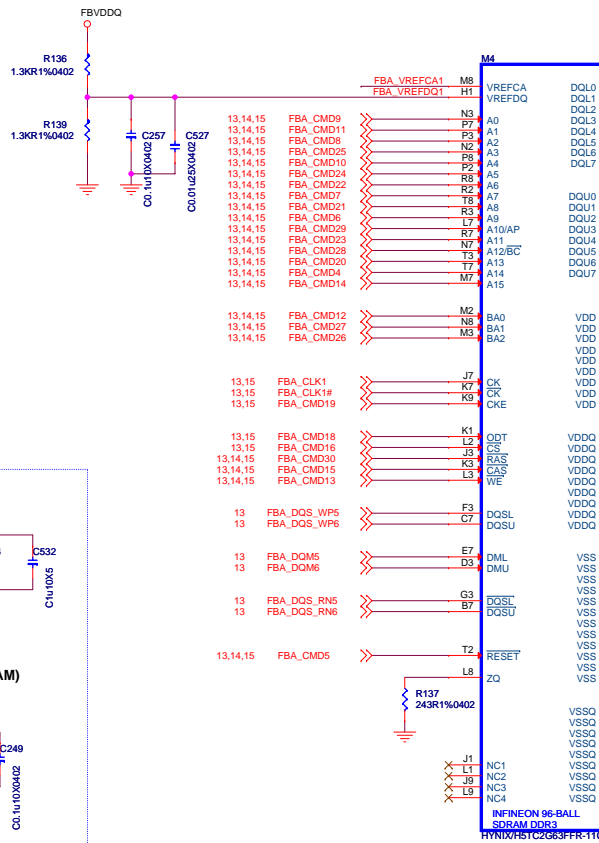
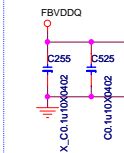




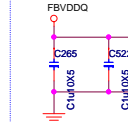
Under VRAM



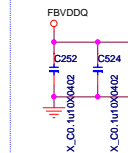
2 x 0.1u
4 x 1u
(per VRAM)



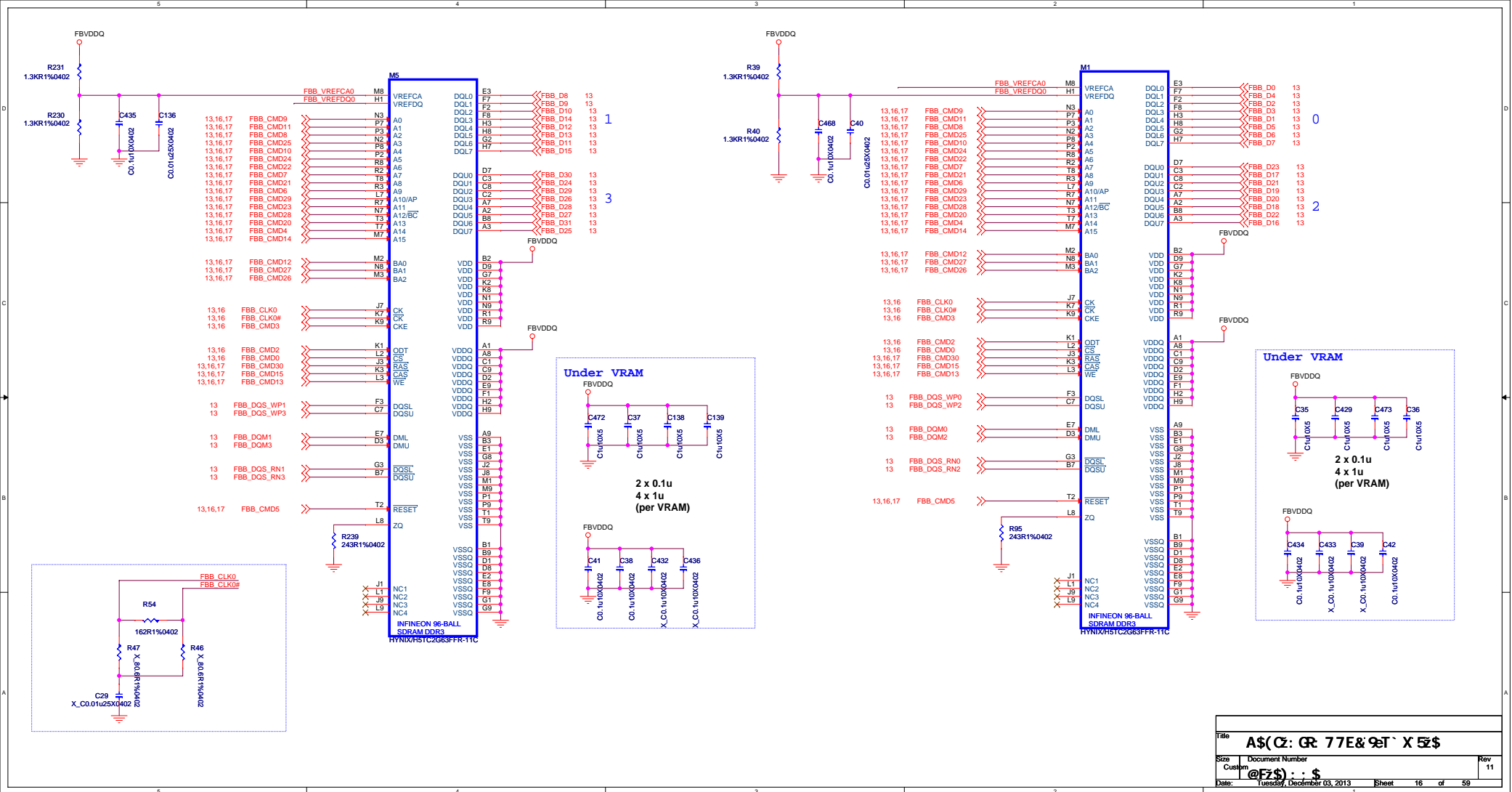
Under VRAM

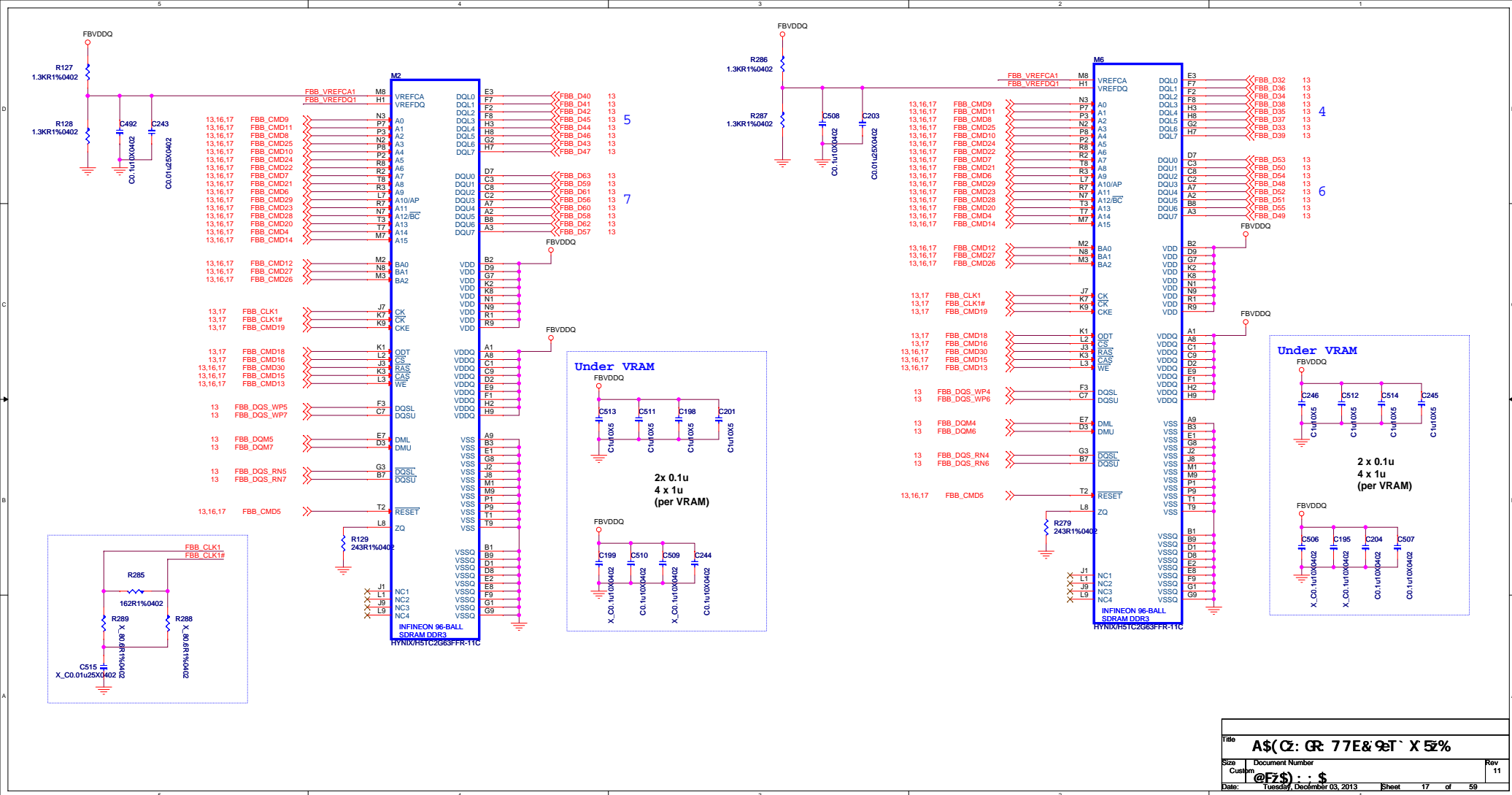


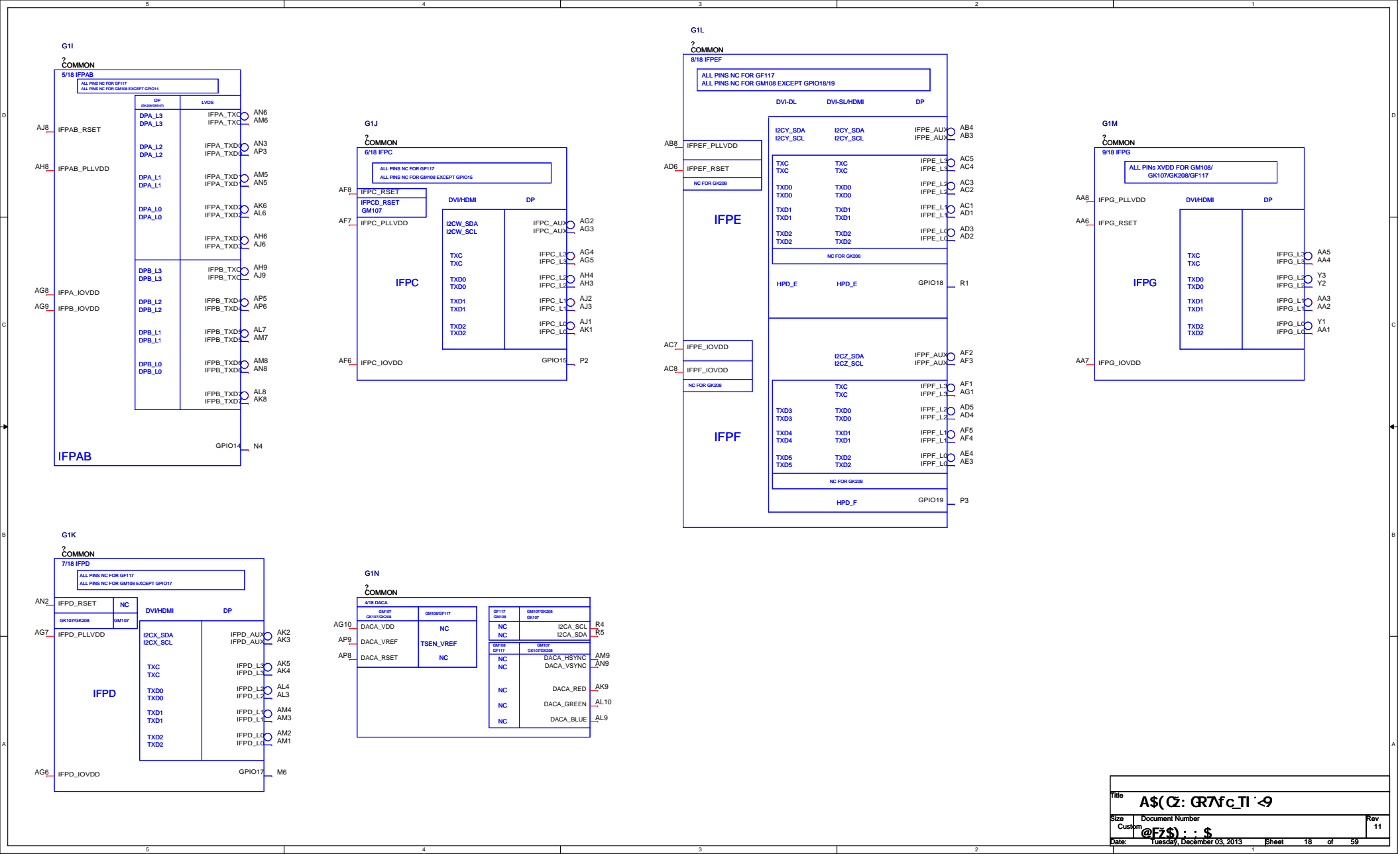
2 x 0.1u
4 x 1u
(per VRAM)



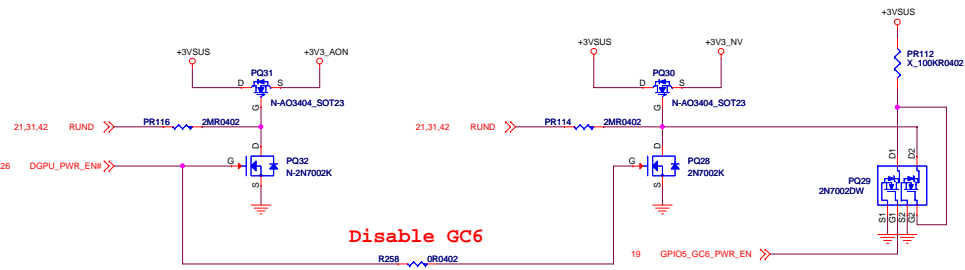
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Size	Document Number		Rev
Custom	@Fz\$) : : \$		11
Date:	Tuesday, December 03, 2013	Sheet	15 of 59



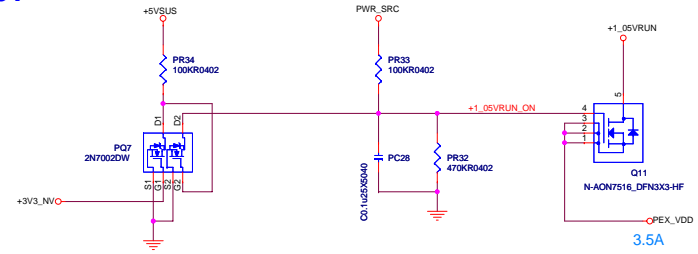




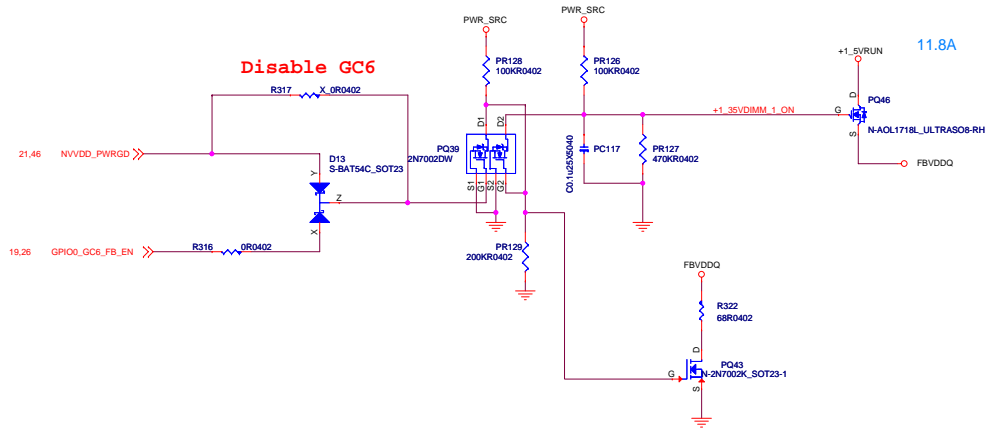
3.3V



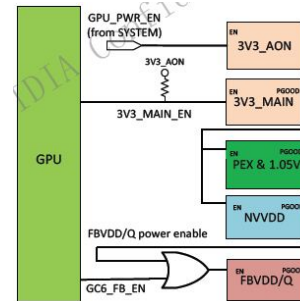
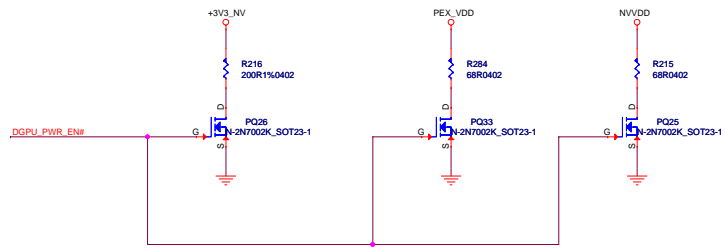
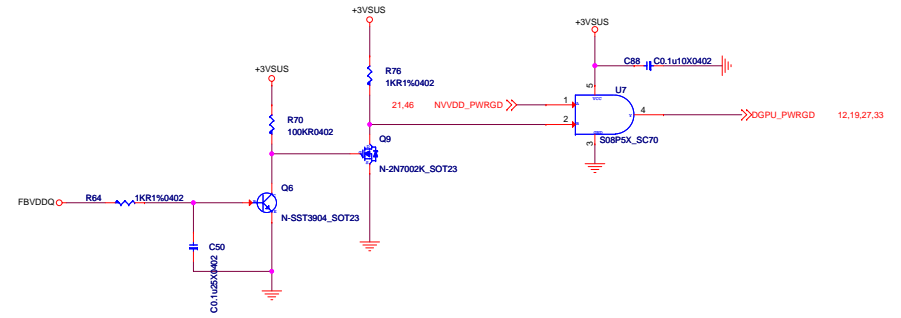
1.05V



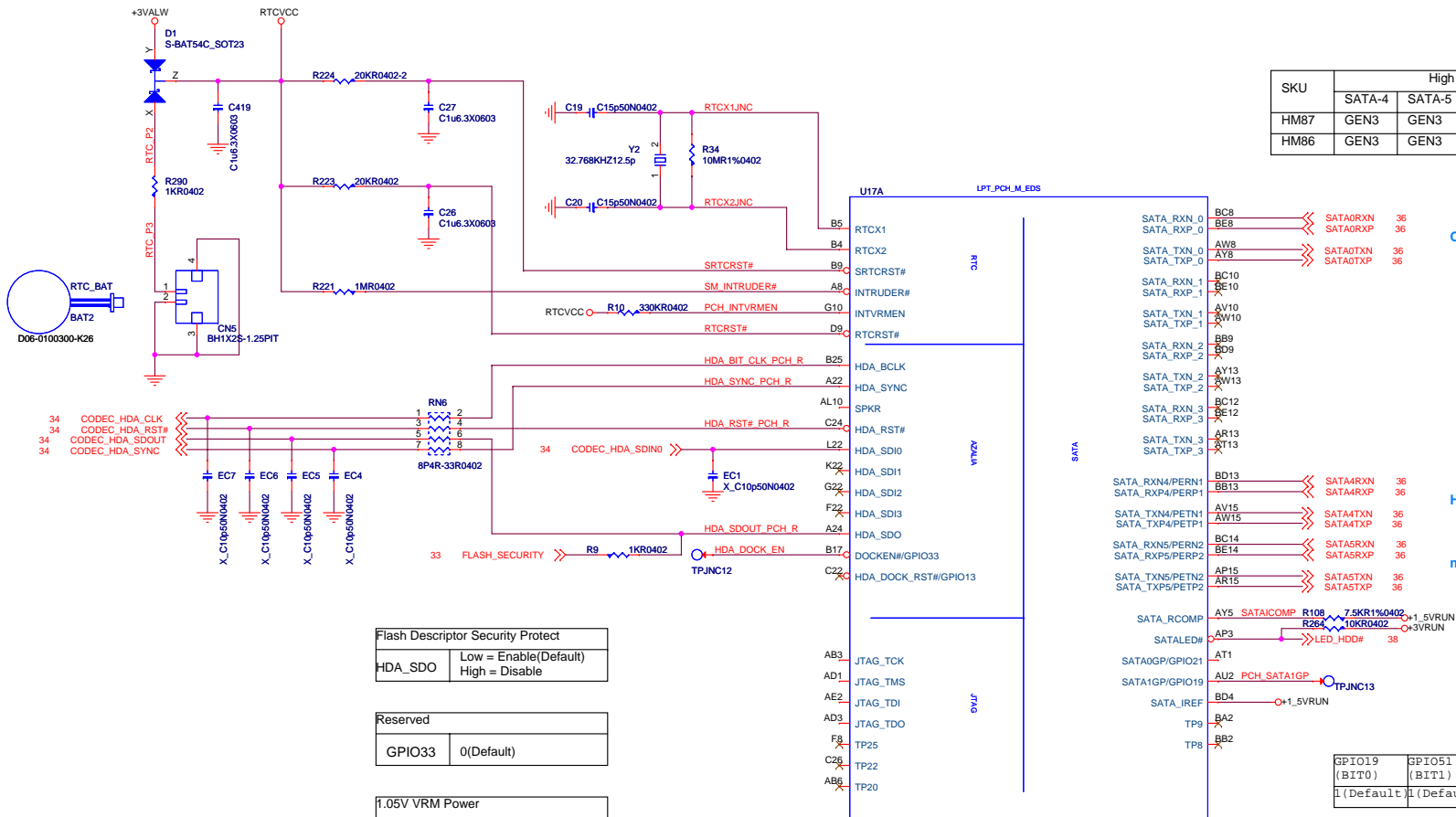
1.5V



GPU_PWRGD



Title			
AS/ G: GRChj Xe 6bagsb			
Size	Document Number	Rev 11	
Custom	@Fz\$) : : \$		
Date:	Tuesday, December 03, 2013	Sheet	21 of 59



SKU	High Speed SATA I/O Ports					
	SATA-4	SATA-5	SATA-0	SATA-1	SATA-2	SATA-3
HM87	GEN3	GEN3	GEN3	GEN3	GEN2	GEN2
HM86	GEN3	GEN3	GEN2	N/A	GEN2	N/A

ODD — SATA GEN2

HDD — SATA GEN3

m-SATA — SATA GEN3

GPIO19 (BIT0)	GPIO51 (BIT1)	BIOS
1(Default)	1(Default)	SPI

Title		
C6: 7\$fl: 7.4"-G4: "F4G4"fl		
Size	Document Number	Rev
Customer	@Fz\$)	10
Date:	Tuesday, December 03, 2013	Sheet 22 of 59

For 175A

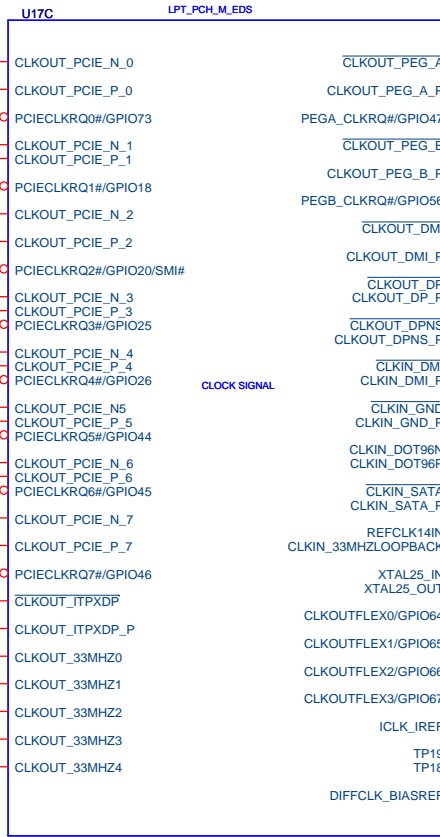
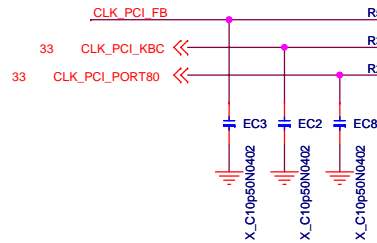
39 CLK_PCIE_CARD1#
39 CLK_PCIE_CARD1
39 CARDREADER1_CLKREQ#

For 16GH

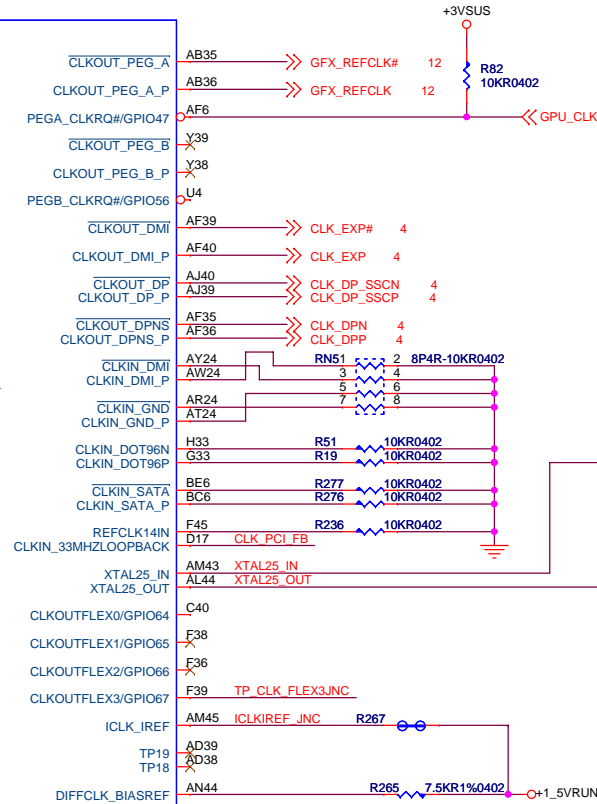
35 CLK_PCIE_CARD2#
35 CLK_PCIE_CARD2
35 CARDREADER2_CLKREQ#
39 CLK_PCIE_LAN#
39 CLK_PCIE_LAN
39 GLAN_CLKREQ#
31 CLK_ANX1122_N
31 CLK_ANX1122_P

[Fuqun]CLK1/2: RUN
CLK0/3/4/5/6/7: SUS

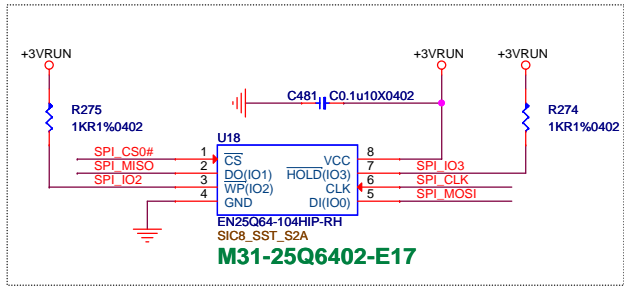
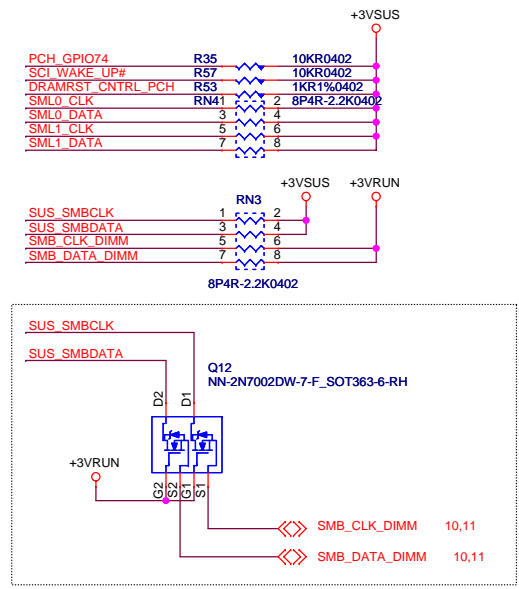
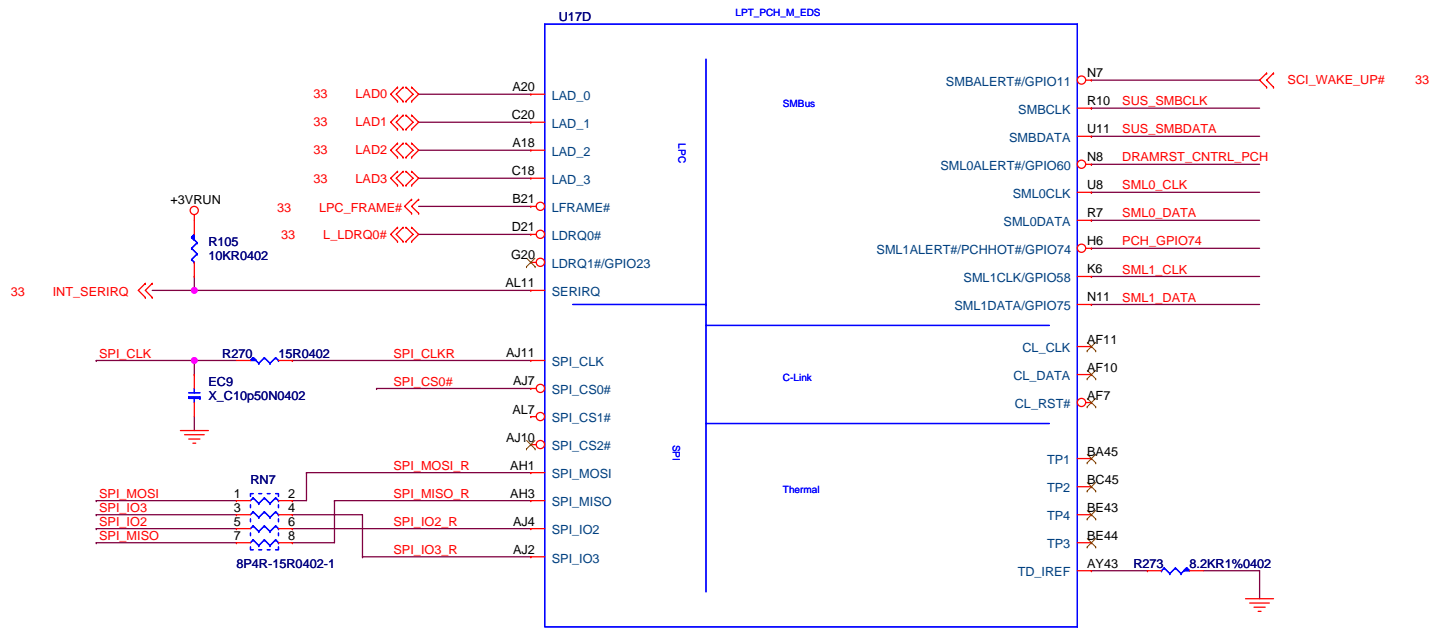
Reserved	
GPIO44	1(Default)
GPIO46	1(Default)



CLOCK SIGNAL



Title		
C6: 7%fl 6?> fl		
Size	Document Number	Rev
Custom	@Fz\$)	11
Date:	Tuesday, December 03, 2013	Sheet 23 of 59



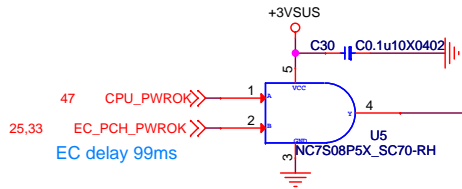
+3VSUS

R38 10KR0402 SUSPWACK
R6 10KR0402 AC_PRESENT
R59 10KR0402 PM_RI#
R49 8.2KR1% PM_BATLOW#
R248 10KR0402 PCIE_WAKE#

[Fuqun] WAKE# PU 1K in checklist

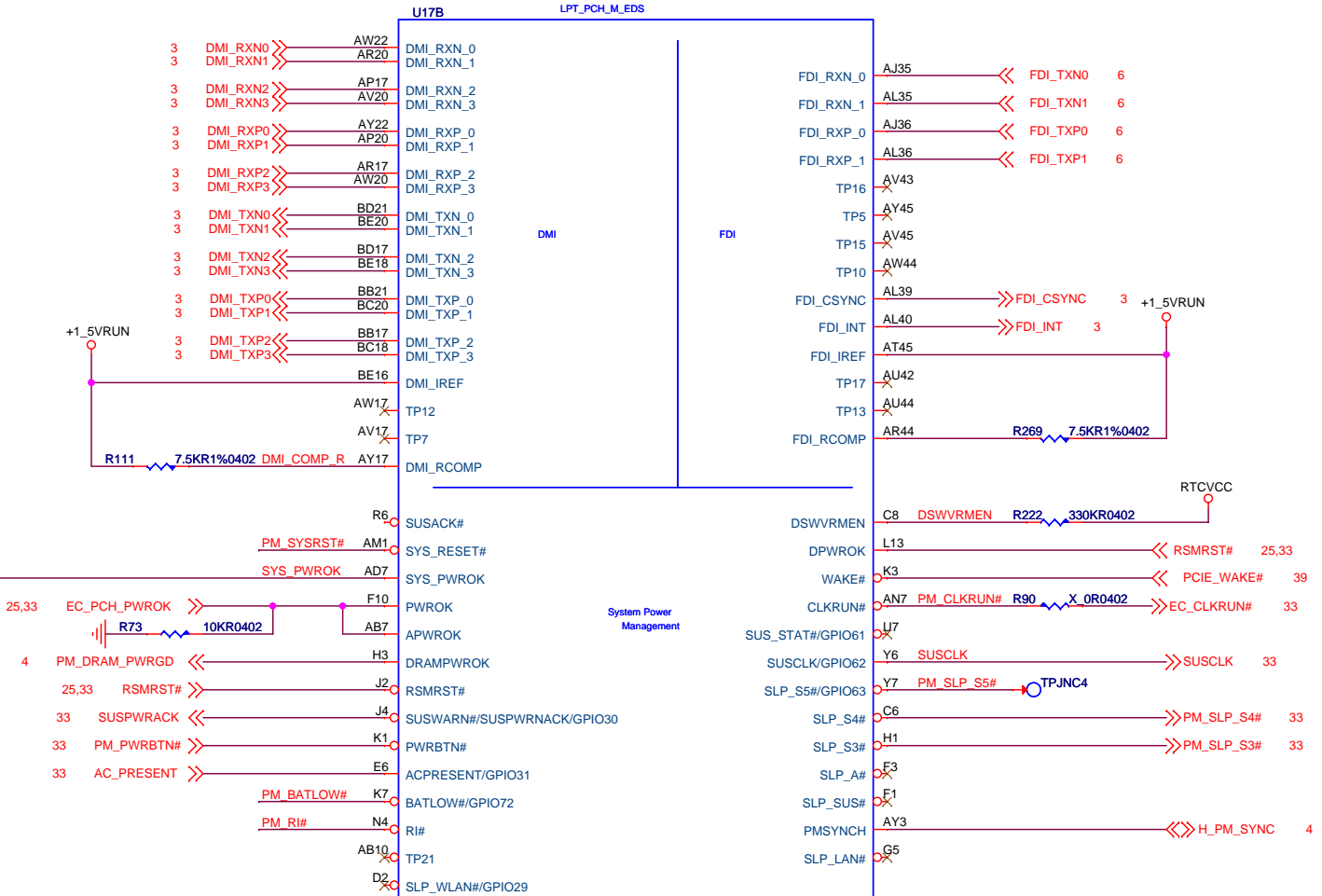
+3VRUN

R91 8.2KR0402 PM_CLKRUN#
R26 10KR0402 PM_SYSRST#



PLL On-Die Voltage Regulator Enable	
SUSCLK	0 =Disable 1 = Enable(Default)

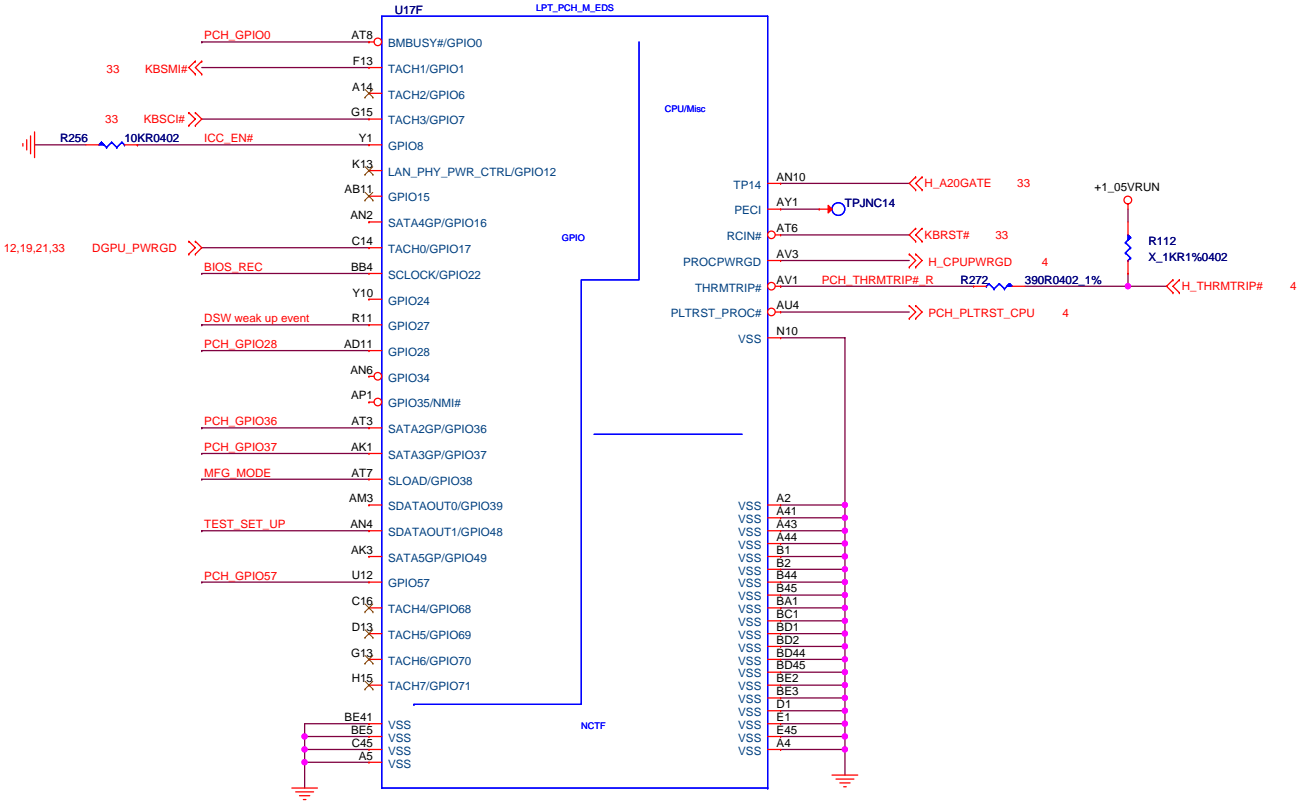
Deep Sx On-Die Voltage Regulator Enable	
DSWVRMEN	0 =Disable 1 = Enable



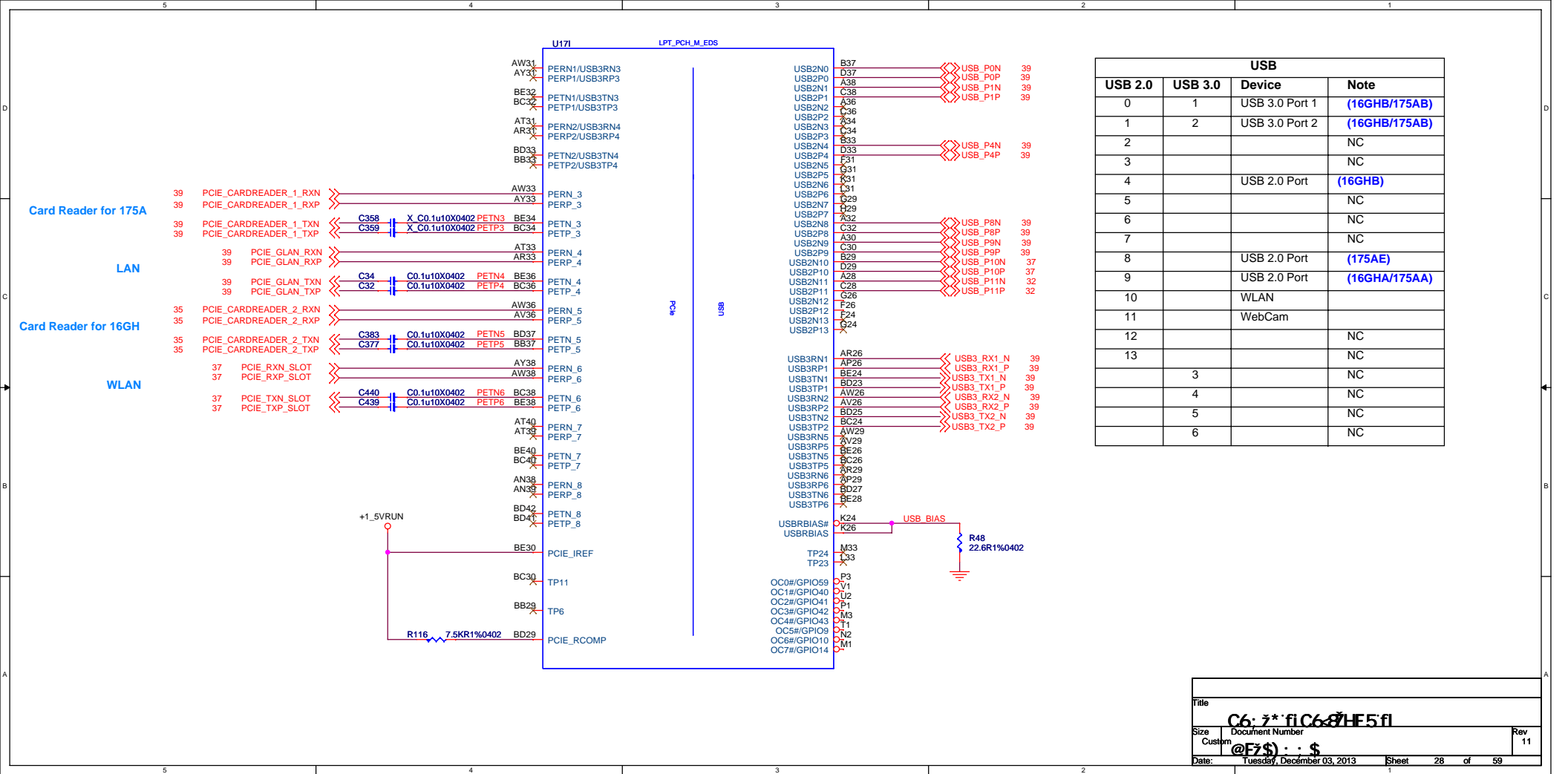
Title		
C6; ž' fi 7 @ž97<fi		
Size	Document Number	Rev
Custom	@F7\$) : : \$	11
Date:	Tuesday, December 03, 2013	Sheet 25 of 59

GPIO Setting : Ref 486708_LPT_EDS Section2.24

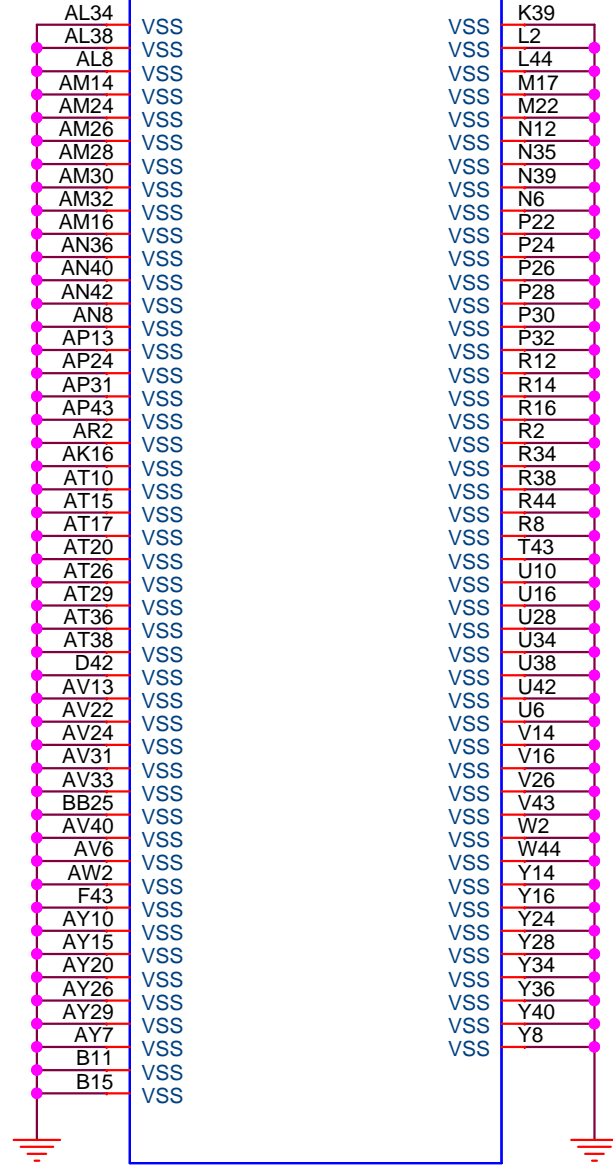
PLL ON DIE VR_ENABLE	
GPIO28	1=Enable(Default) 0=Disable
Reserved	
GPIO36	0(Default)
TLS	
GPIO37	0=Disable(Default) 1: Enable
Reserved	
GPIO8	1: (Default) 0: CRB



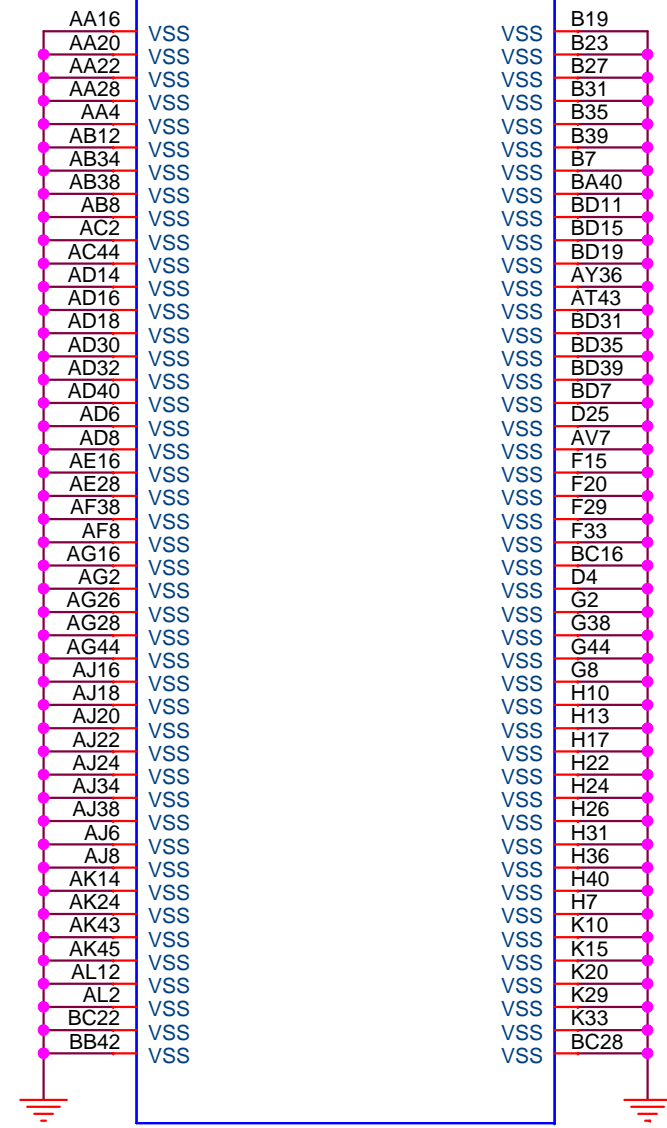
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Size	Document Number	Rev
Custom	1@F\$)	11
Date:	Tuesday, December 03, 2013	Sheet 27 of 59



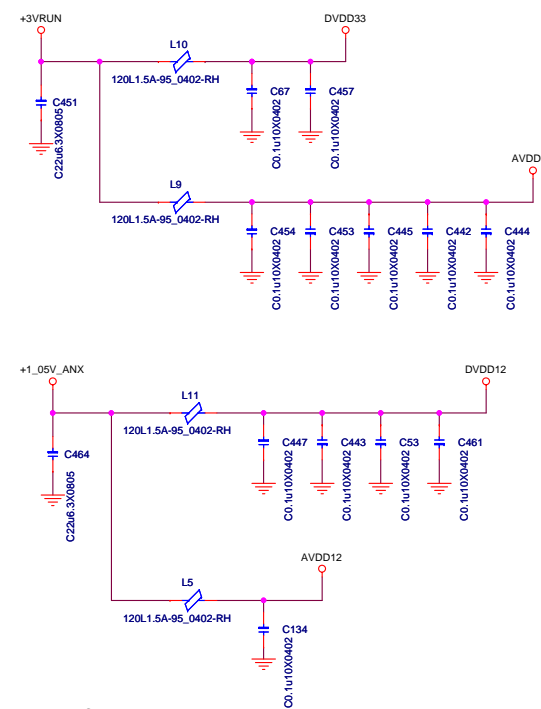
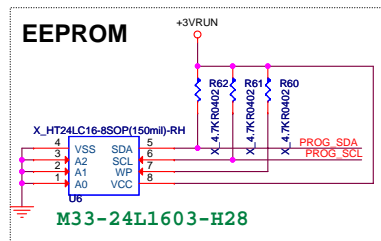
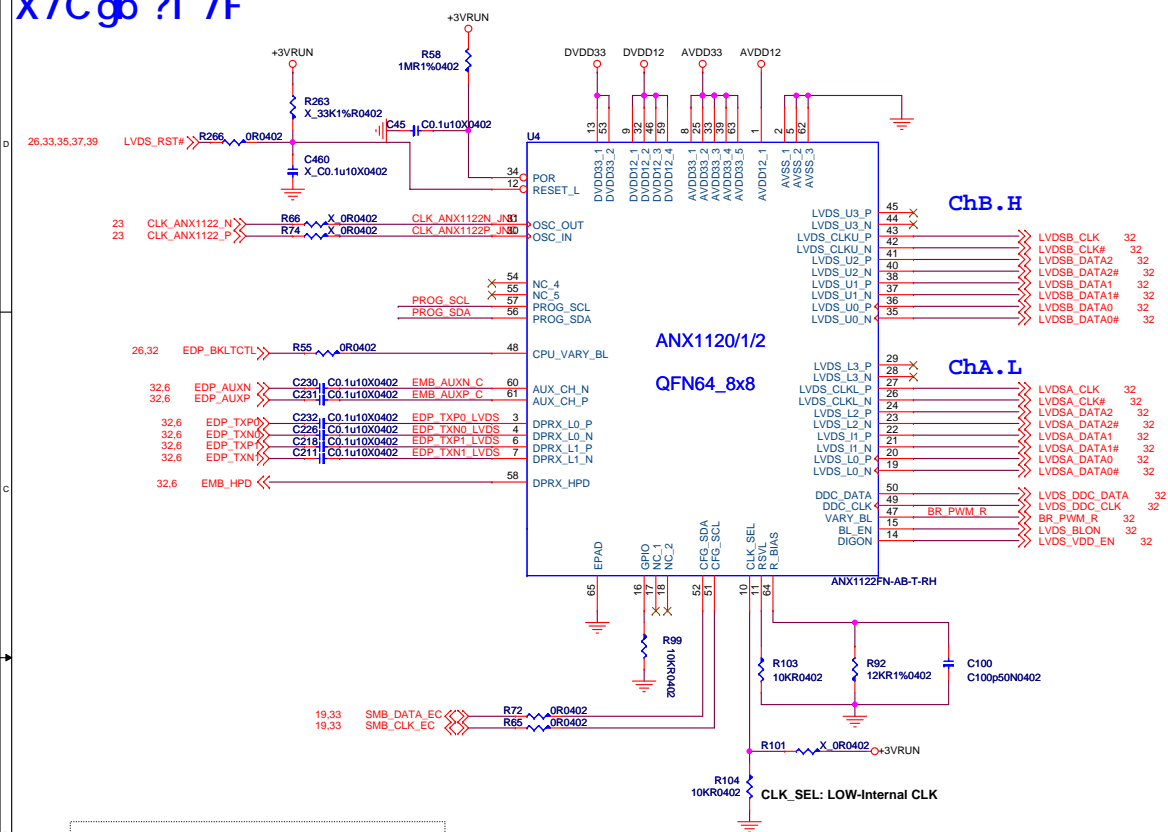
U17J LPT_PCH_M_EDS



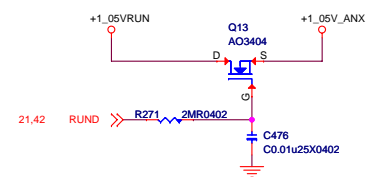
U17K LPT_PCH_M_EDS



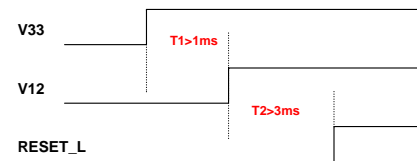
X7Cgb?I 7F

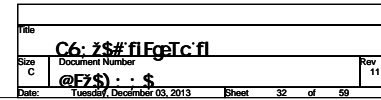


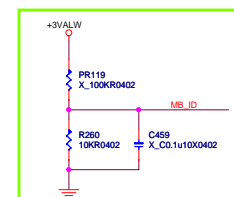
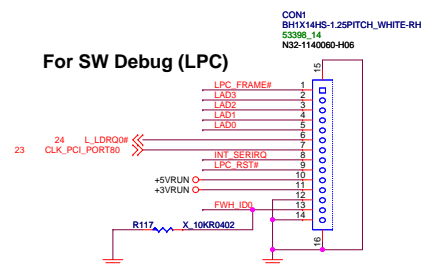
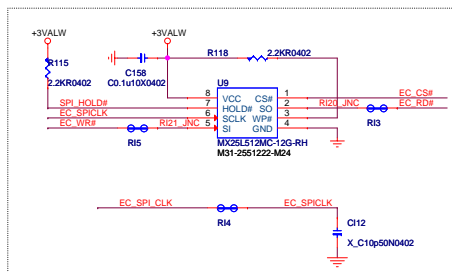
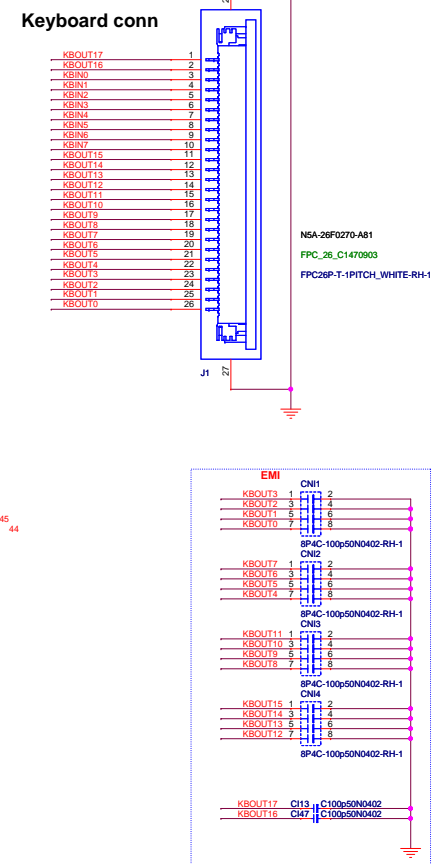
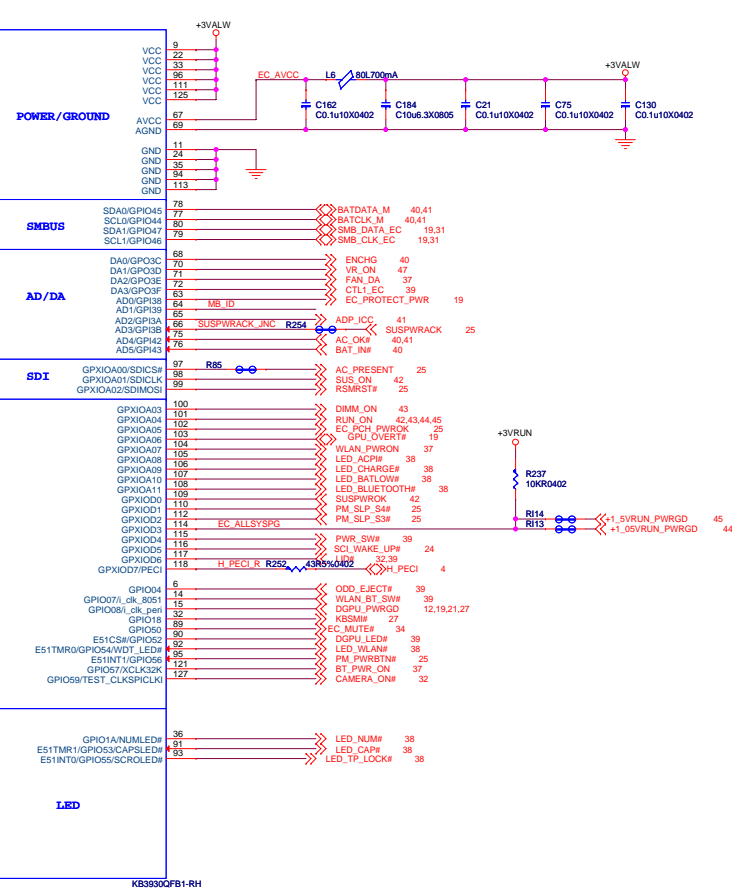
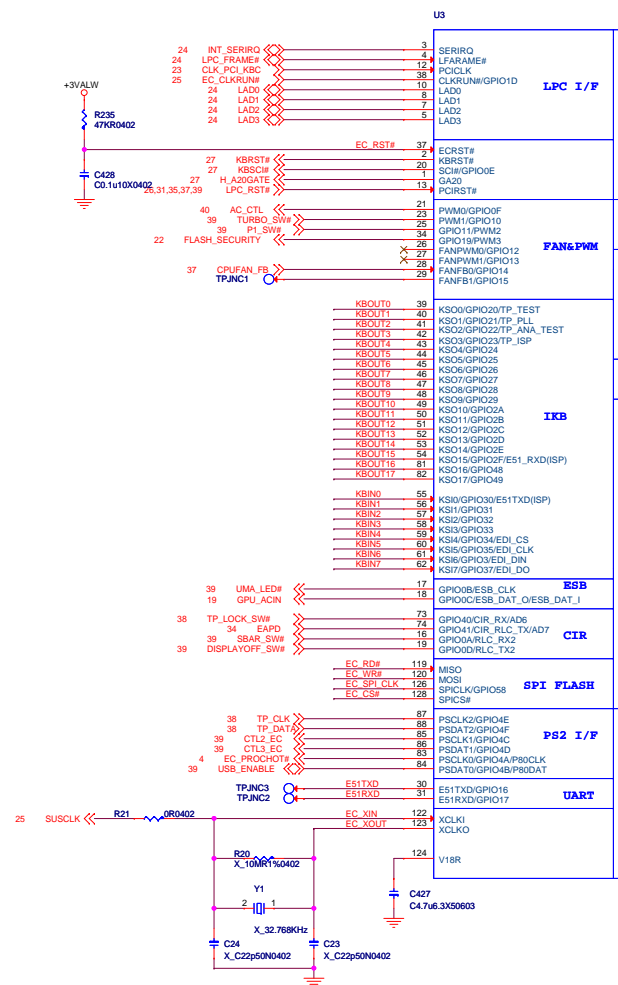
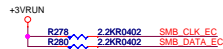
Power on Sequence

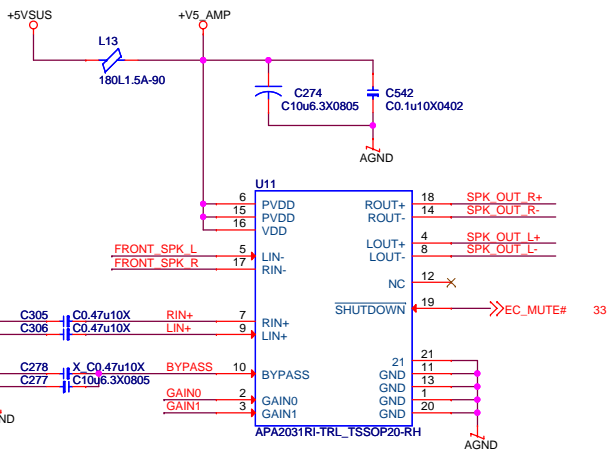
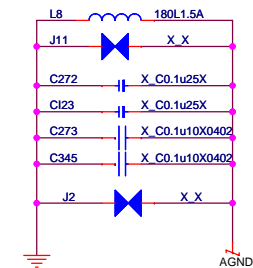
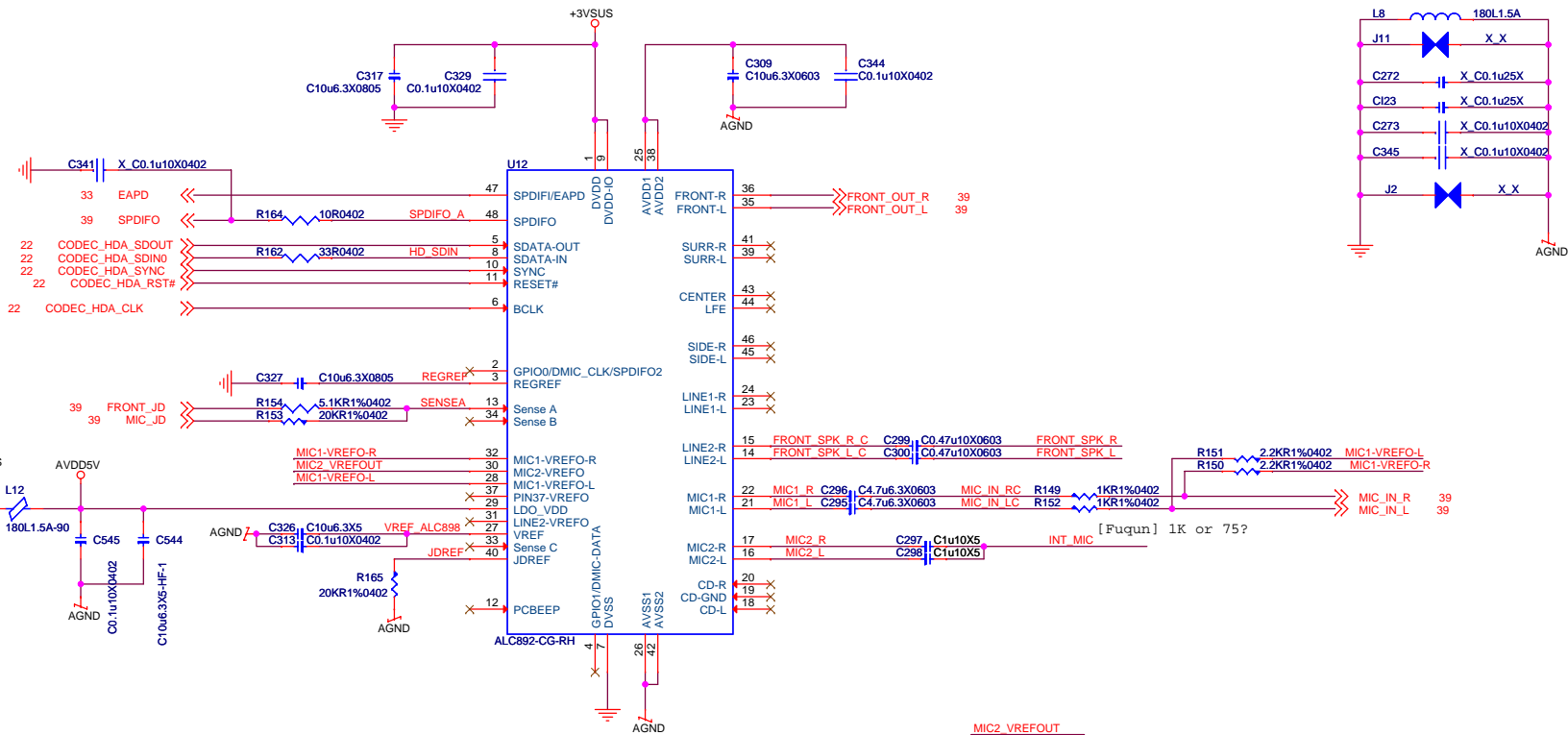


ANX1122 Power on Sequence



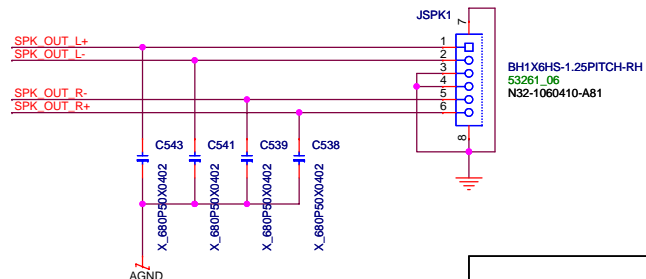
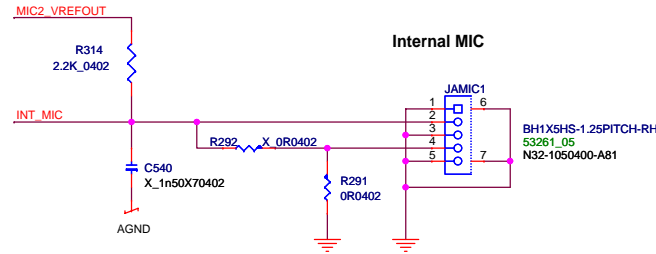
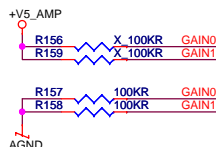


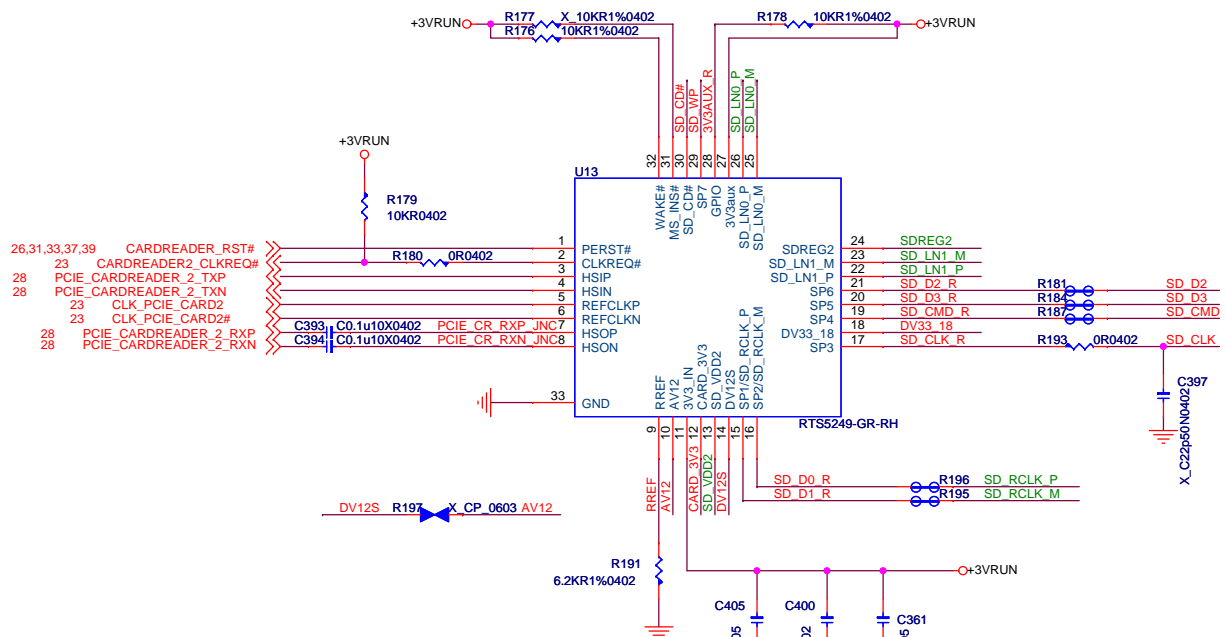




For APA2031

Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X



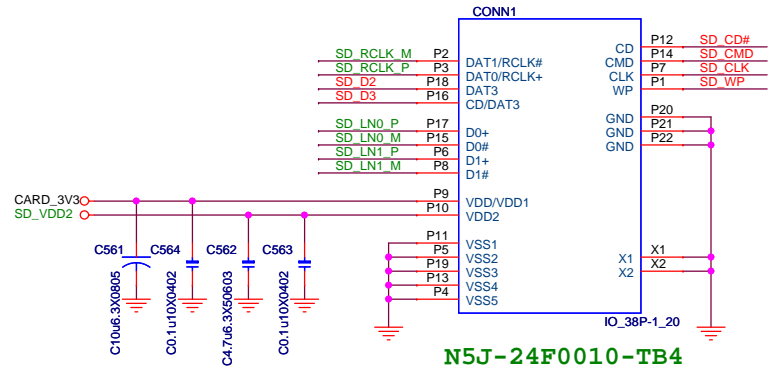
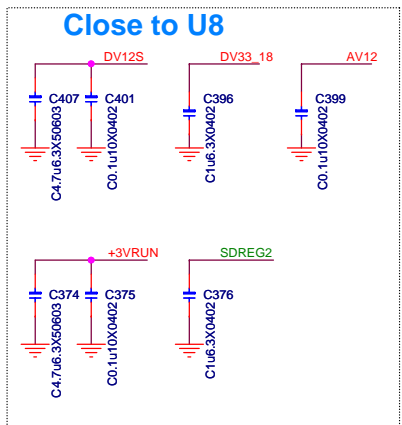


SP1	SD_D1
SP2	SD_D0
SP3	SD_CLK
SP4	SD_CMD
SP5	SD_D3
SP6	SD_D2
SP7	SD_WP

SD_RCLK_M
SD_RCLK_P

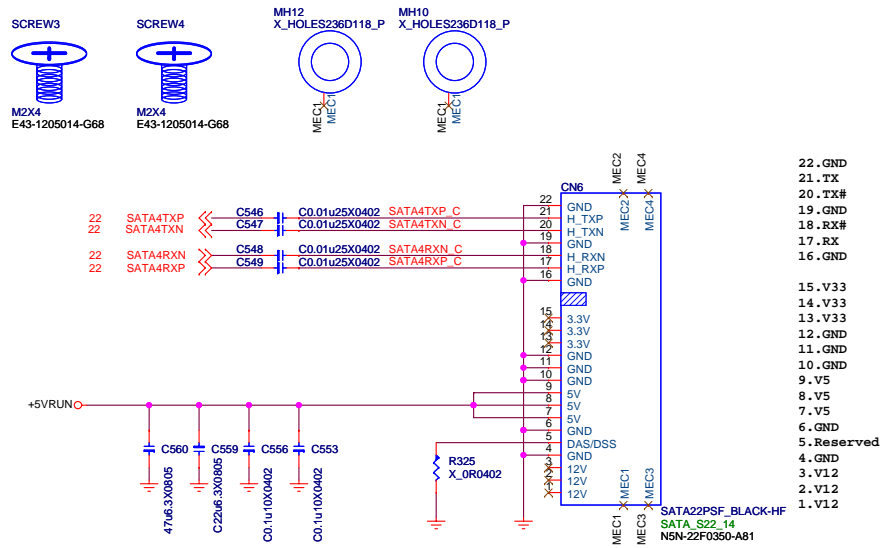
UHS-II

Share Pin

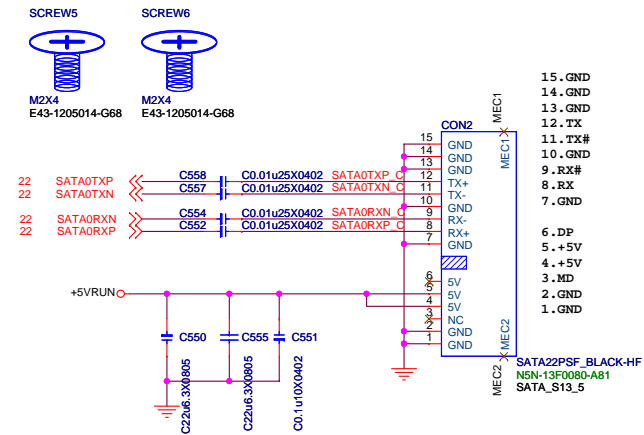


N5J-24F0010-TB4

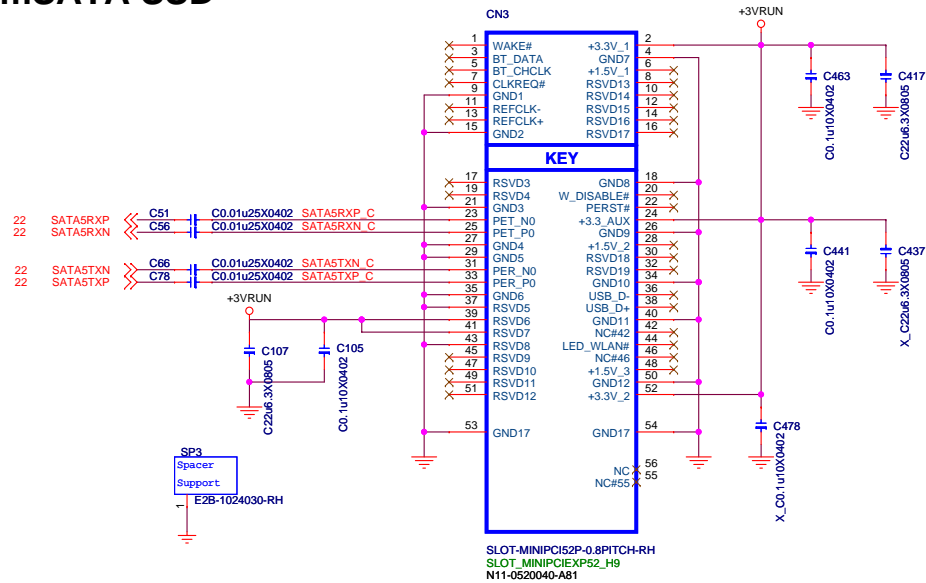
SATA HDD



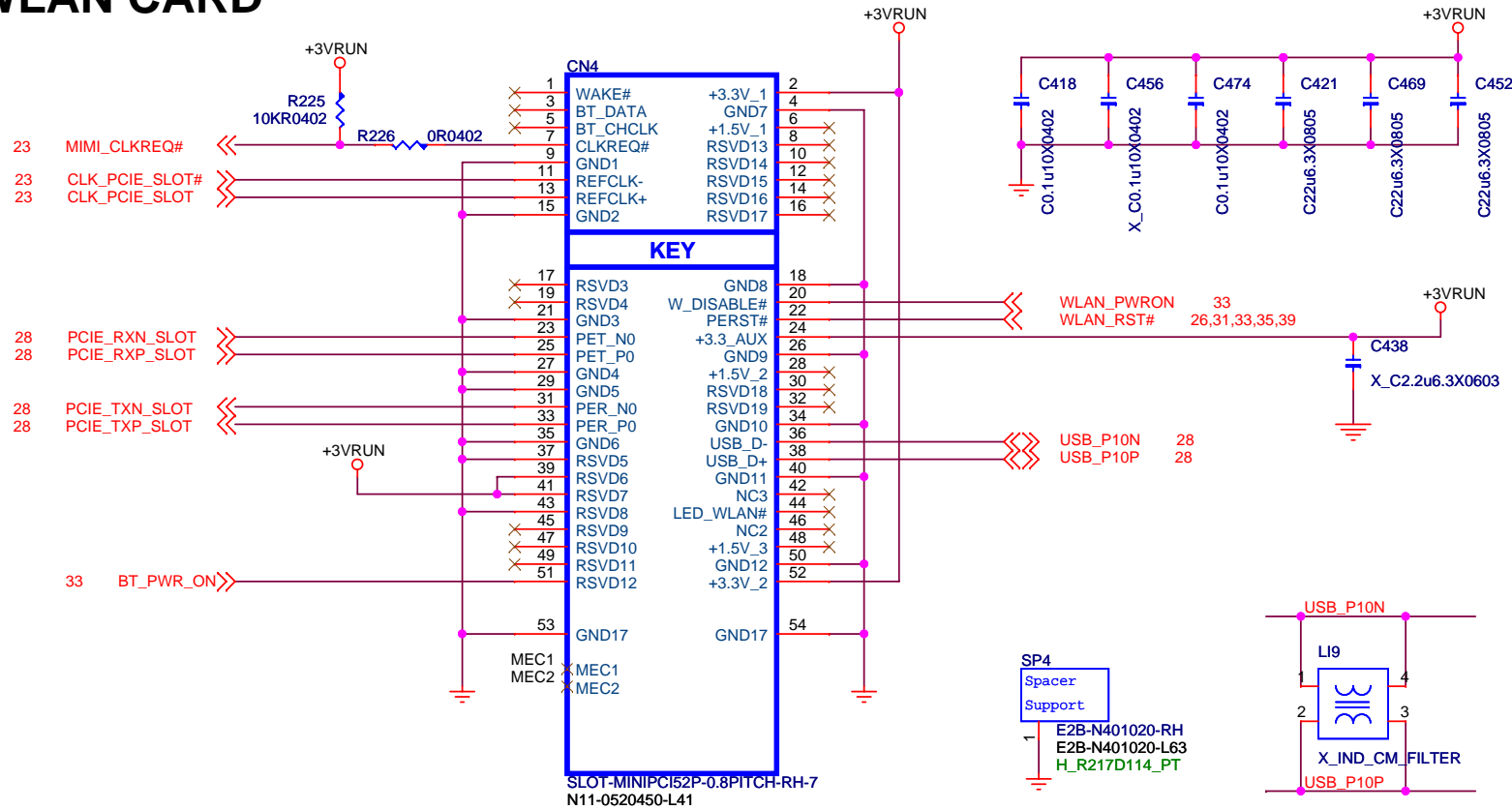
SATA ODD



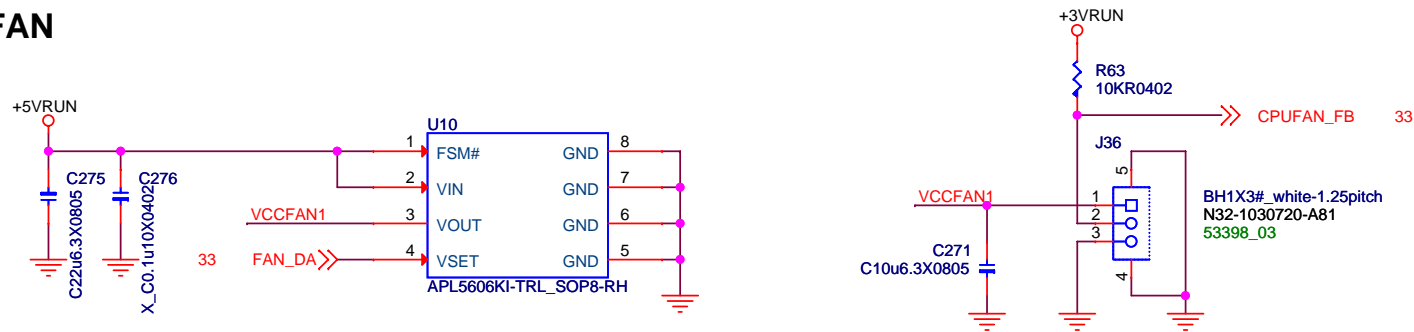
mSATA SSD



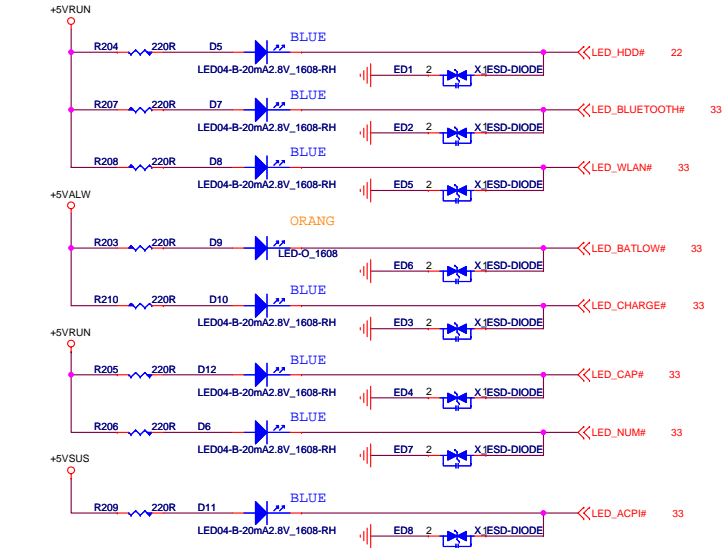
WLAN CARD



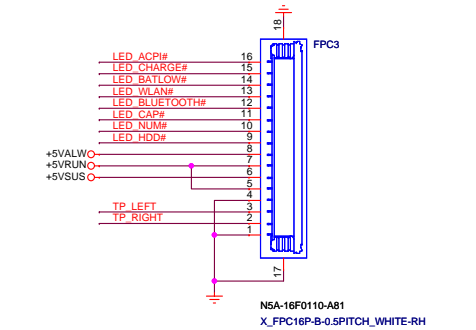
CPU FAN



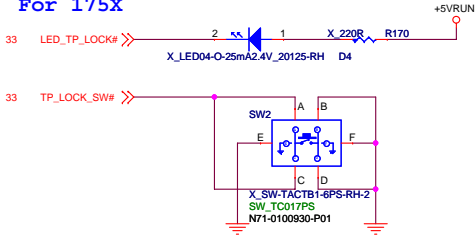
For 16GH



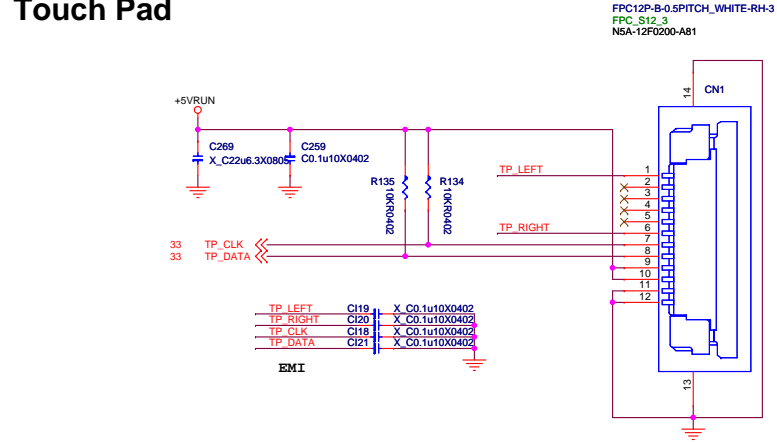
For MS-175AD board



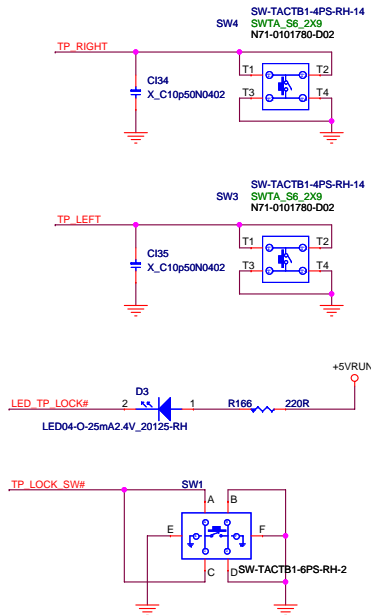
For 175X



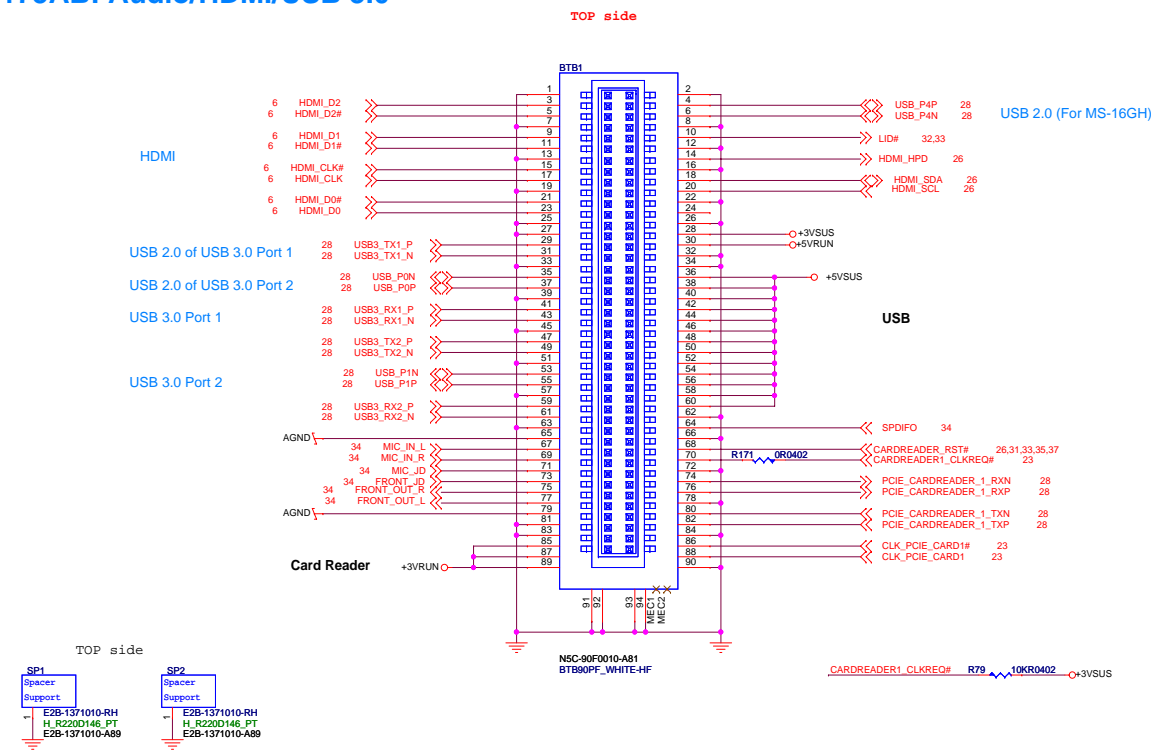
Touch Pad



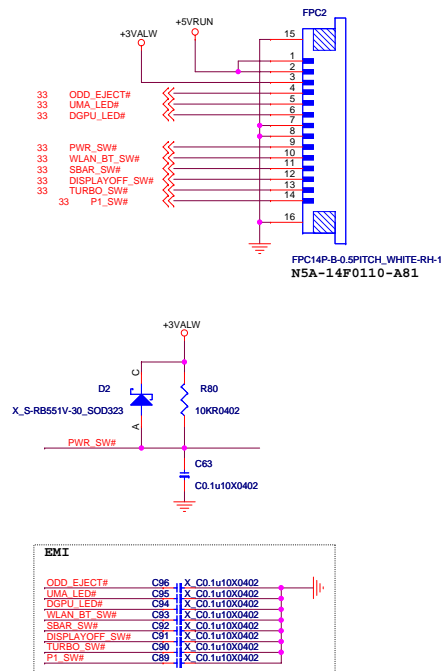
For 16GH



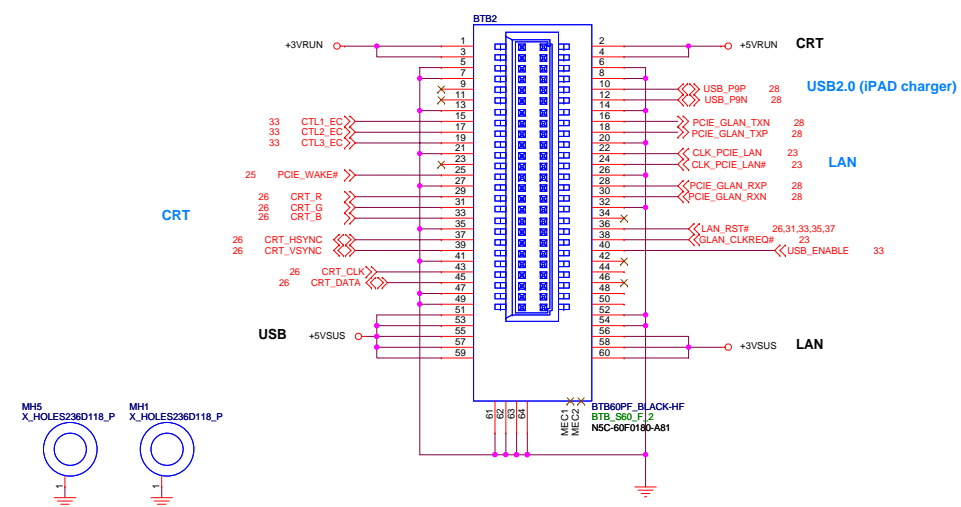
175AB: Audio/HDMI/USB 3.0



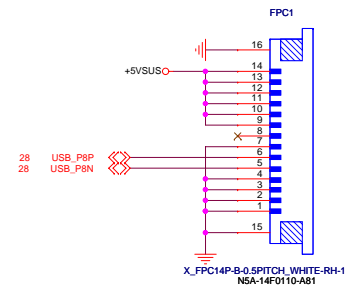
175AC: Power Key Board



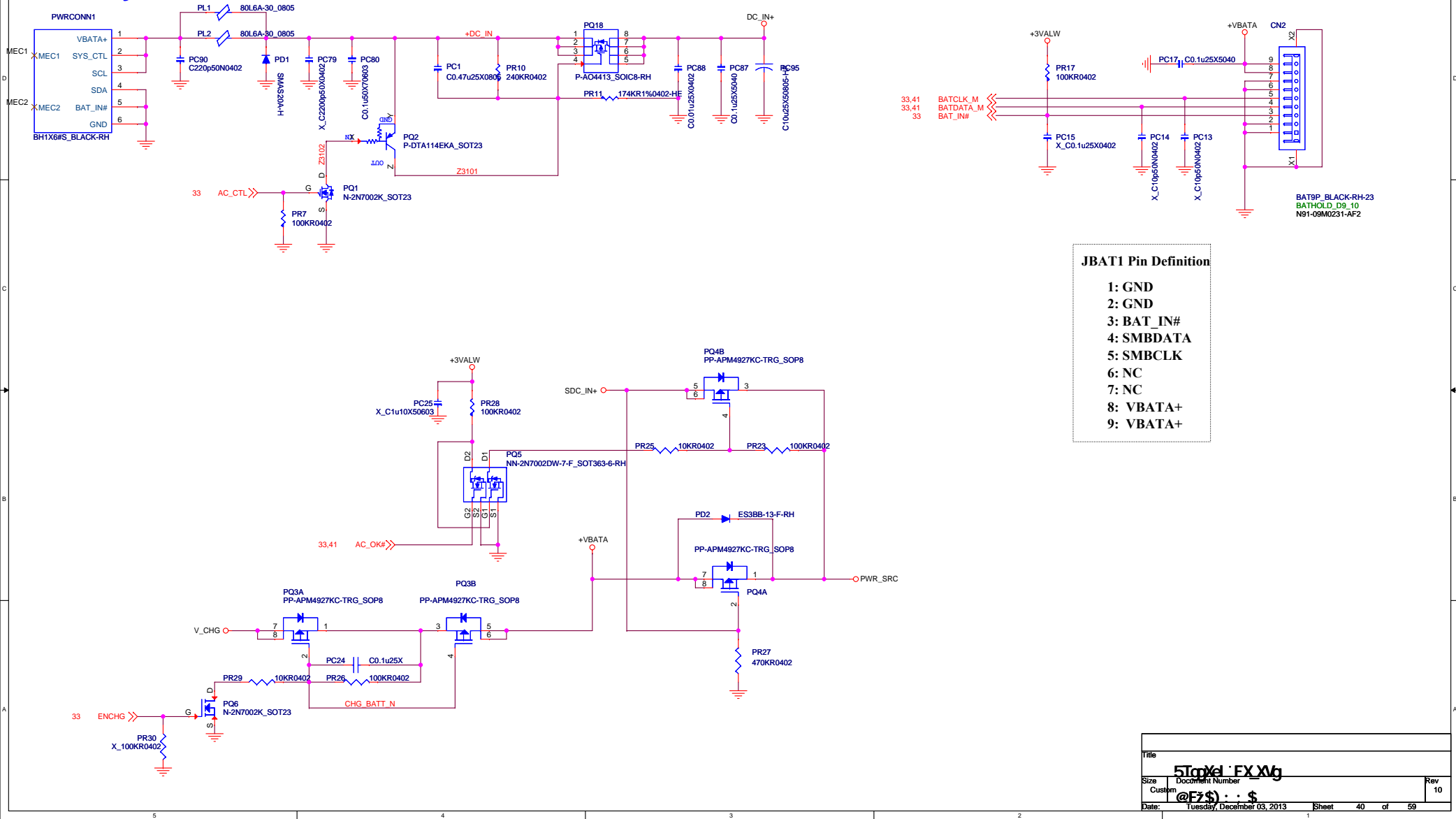
175AA: CRT/USB/WLAN/BT/LAN



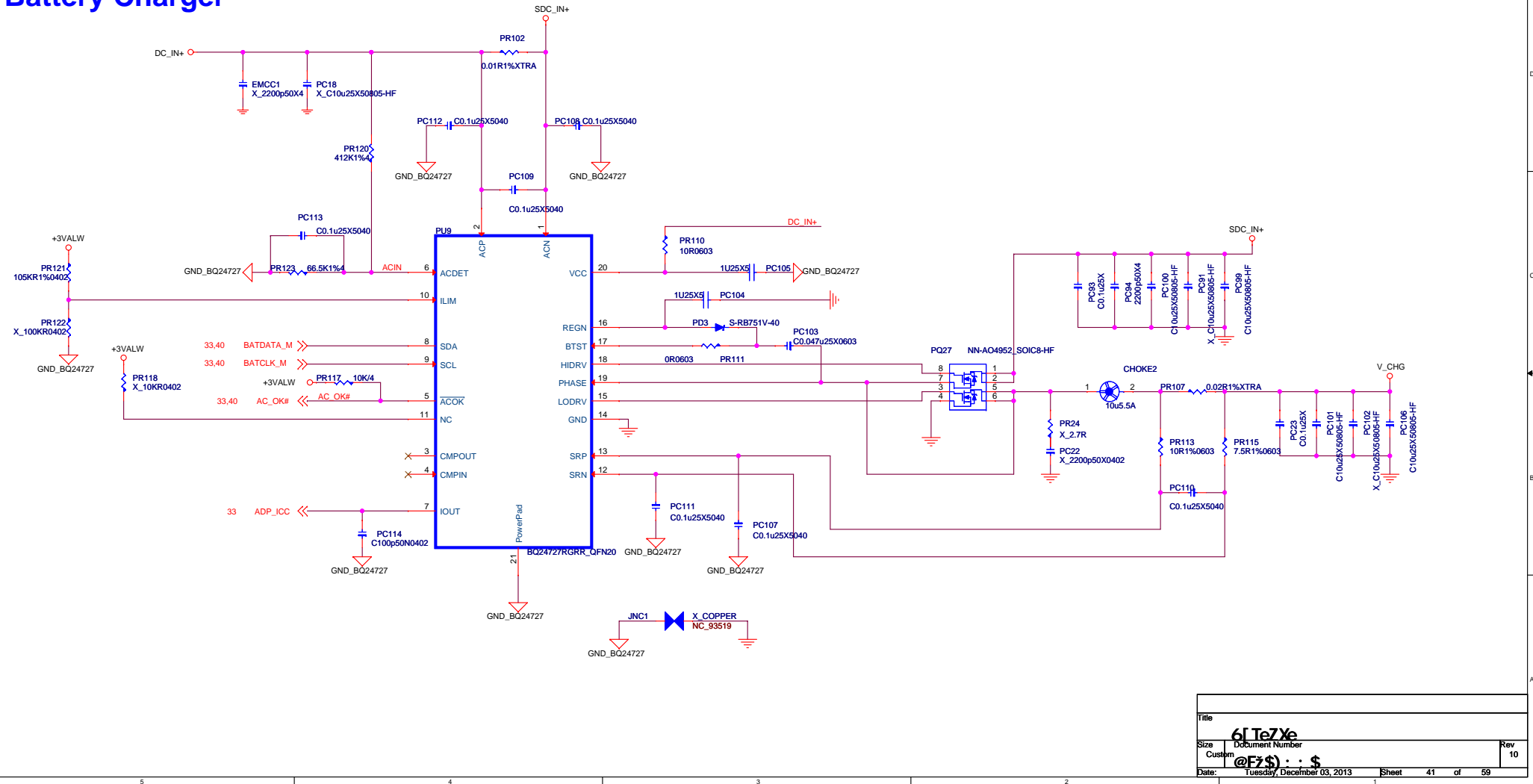
MS-175AE Board



Battery Select

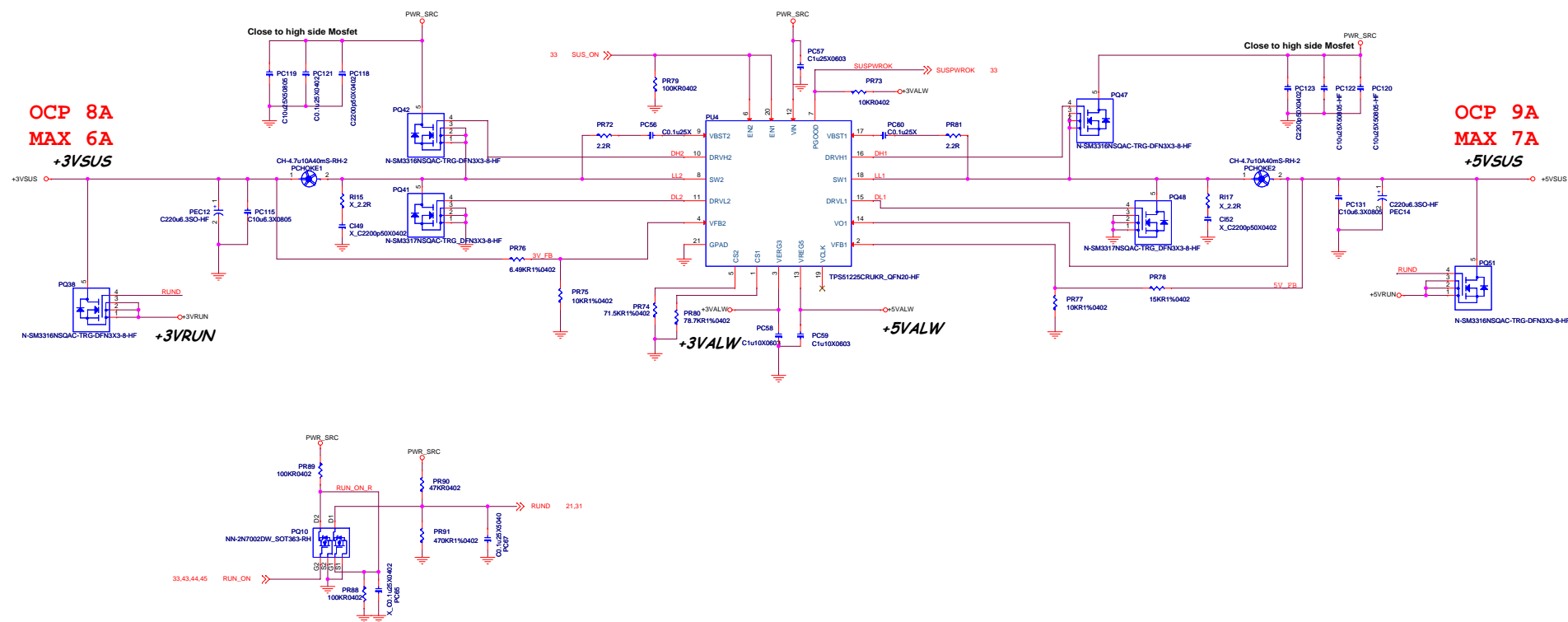


Battery Charger



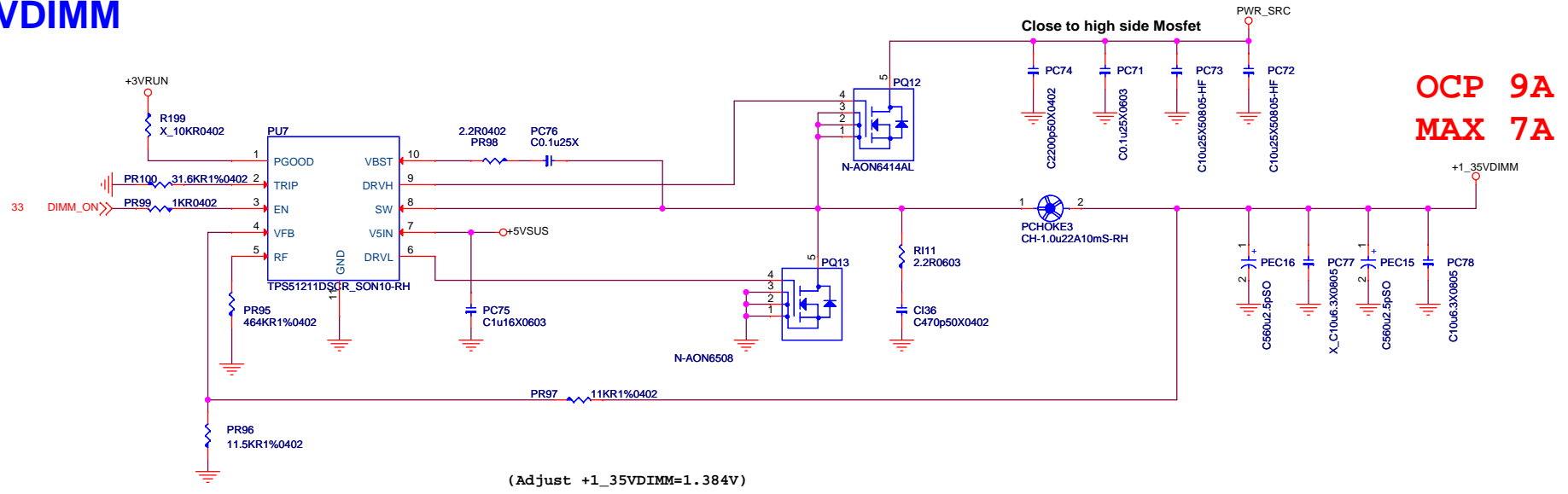
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61 Te7Xe			
Size	Document Number		Rev
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Date:	Tuesday, December 03, 2013	Sheet	41 of 59

System Power

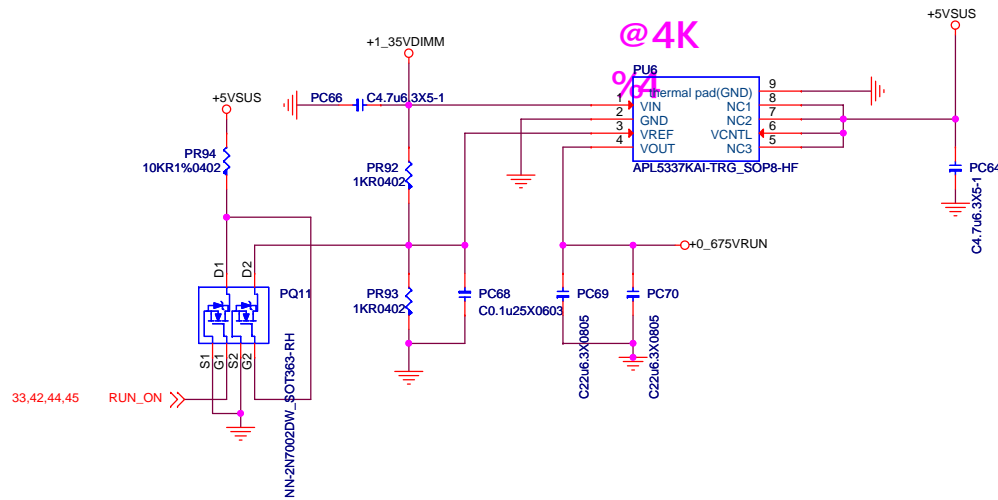


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Date:	Tuesday, December 03, 2013	Sheet	42 of 59

+1.35VDIMM

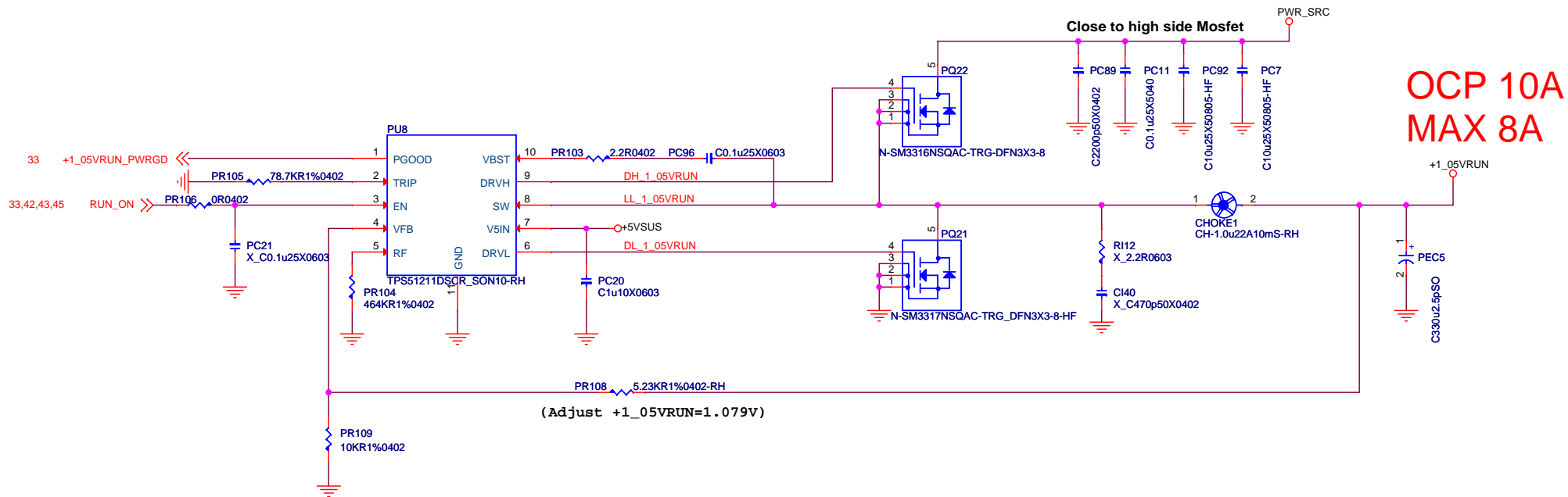


+0.675VRUN



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Date:	Tuesday, December 03, 2013	Sheet 43 of 59

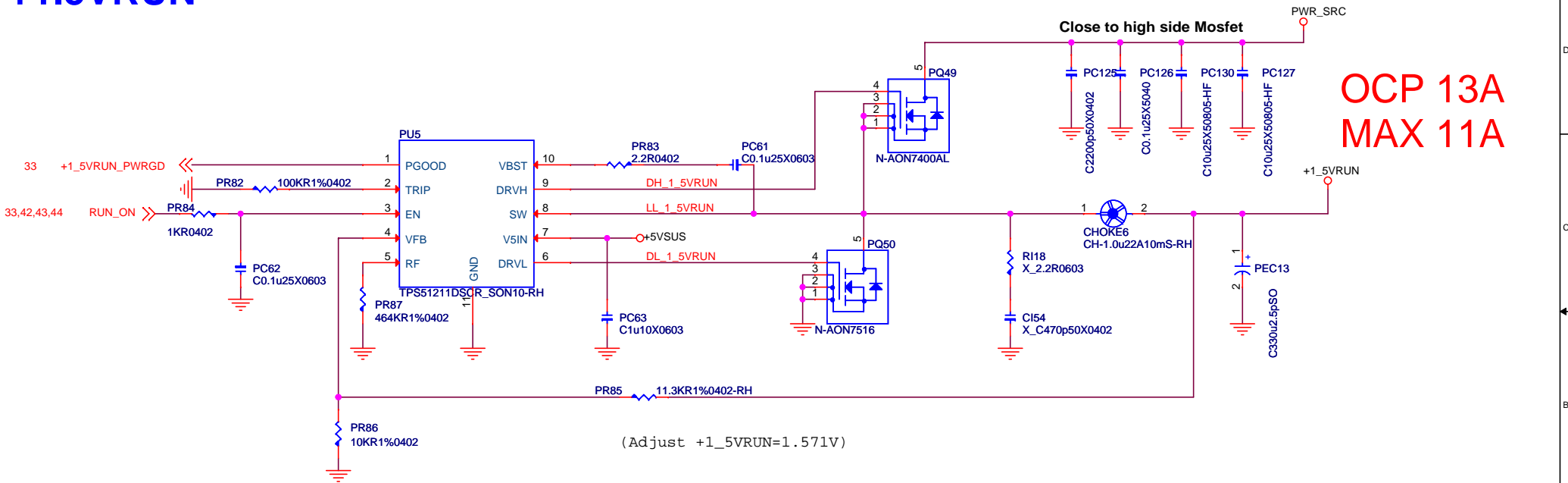
+1.05V RUN



OCP 10A
MAX 8A

Title				
1 \$R#(LEHA				
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Date:	Tuesday, December 03, 2013	Sheet	44 of 59	

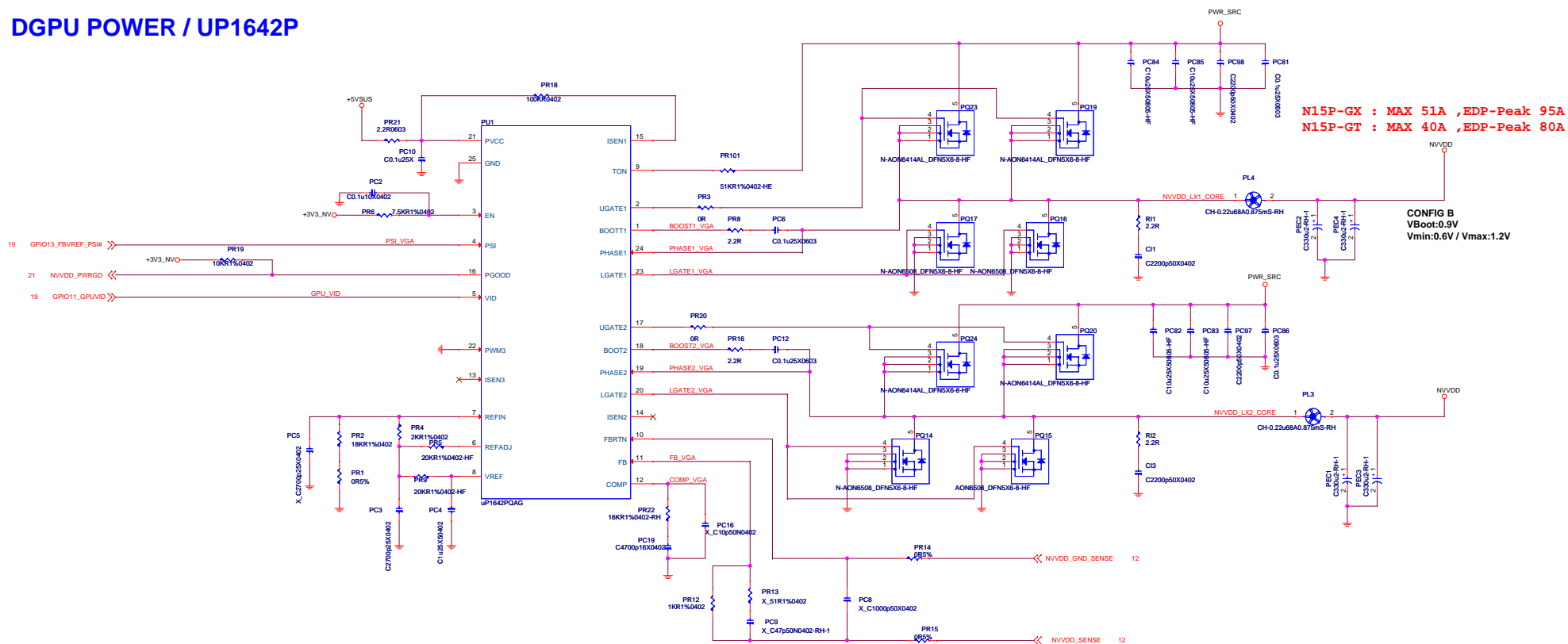
+1.5V RUN



OCP 13A
MAX 11A

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Size	Document Number	
Custom	@F\$) : . \$	
Date:	Tuesday, December 03, 2013	Sheet 45 of 59
Rev		11

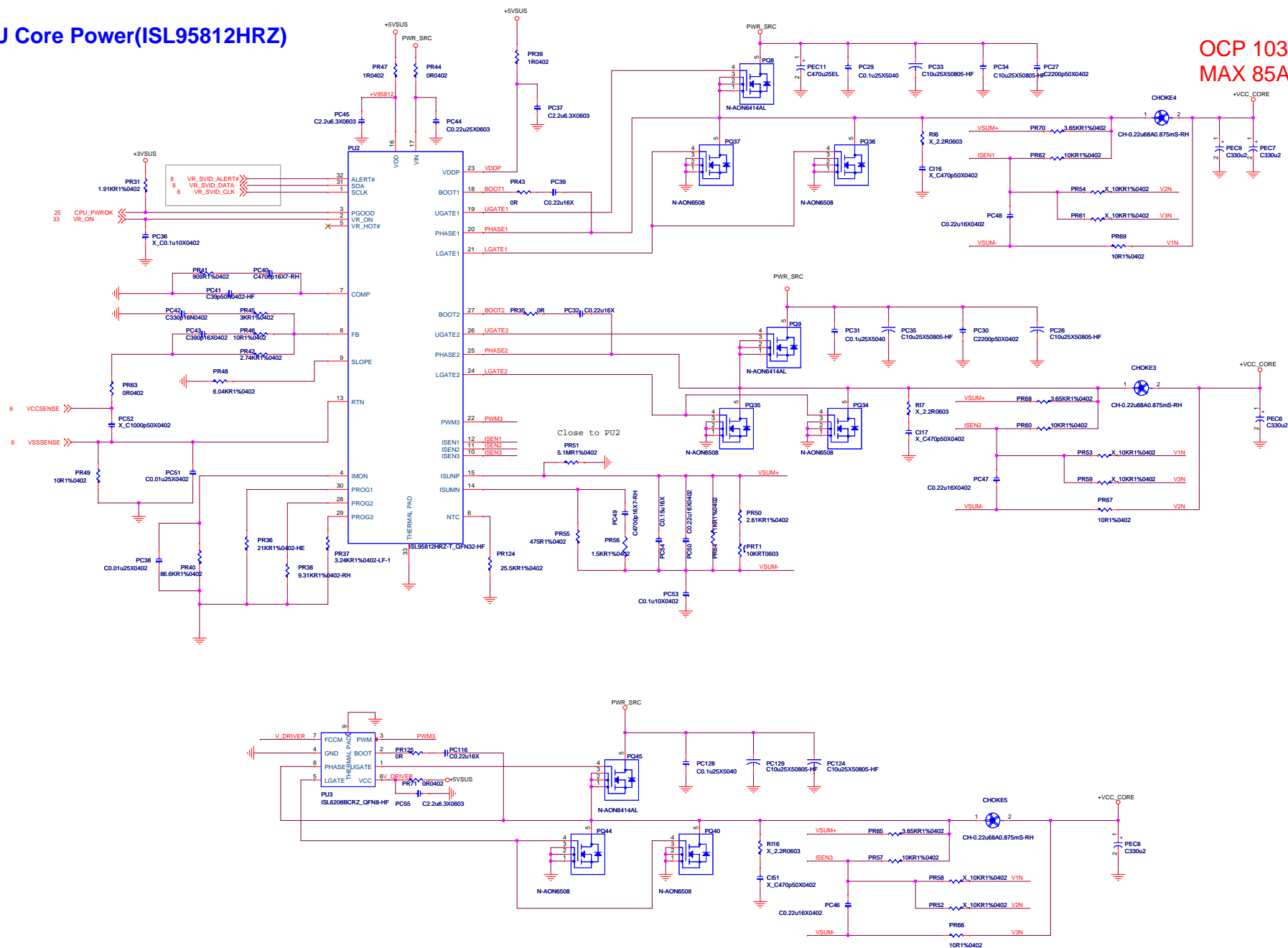
DGPU POWER / UP1642P

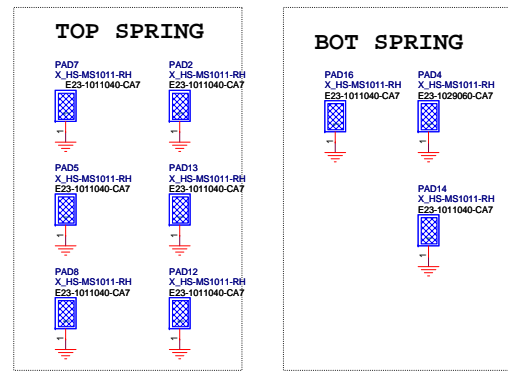
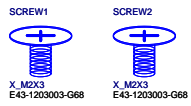
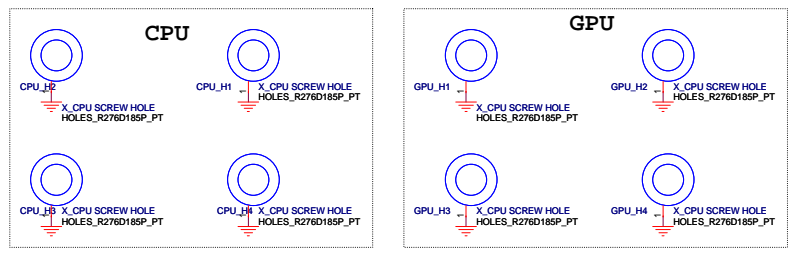
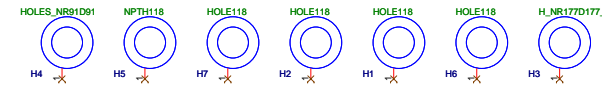
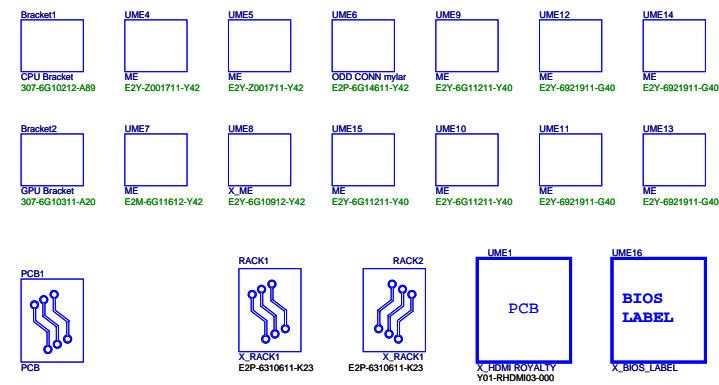
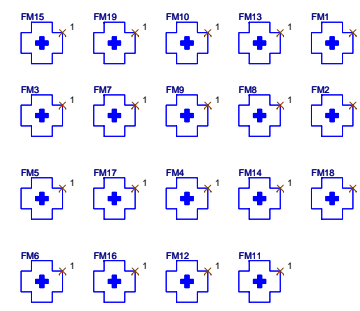
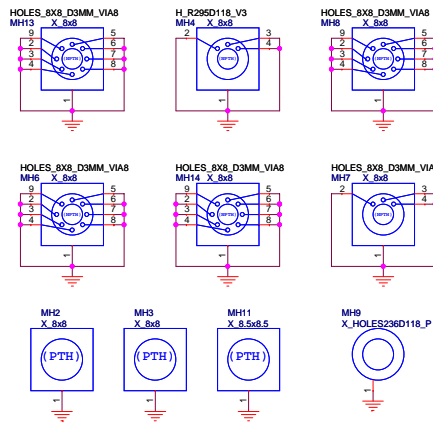


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Date	Tuesday, December 03, 2013
Sheet	46 of 59

CPU Core Power(ISL95812HRZ)

OCP 103A
MAX 85A





Top Spring

PAD6
X_HS-MS1011-RH
E23-1011040-CA7



PAD10
X_HS-MS1011-RH
E23-5551040-CA7



PAD1
X_HS-MS1011-RH
E23-5551040-CA7



BOT Spring

PAD11
X_HS-MS1011-RH
E23-1011040-CA7



PAD15
X_HS-MS1011-RH
E23-1011040-CA7



PAD3
X_HS-MS1011-RH
E23-5551040-CA7

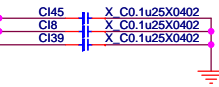


PAD9
X_HS-MS1011-RH
E23-5551040-CA7

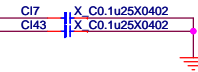


PWR_SRC

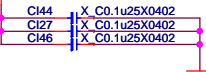
Close to PQ31, PQ34



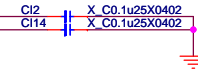
SDC_IN+



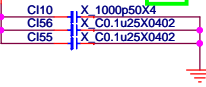
+5VSUS



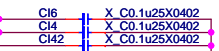
PWR_SRC



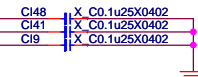
+5VRUN



+VBATA



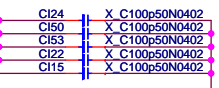
+3VRUN



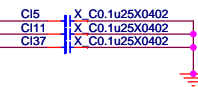
+1.35VDIMM



FBVDDQ

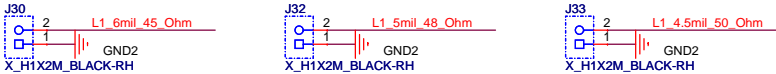


+3VSUS



Single-end

TOP



IN3



IN4

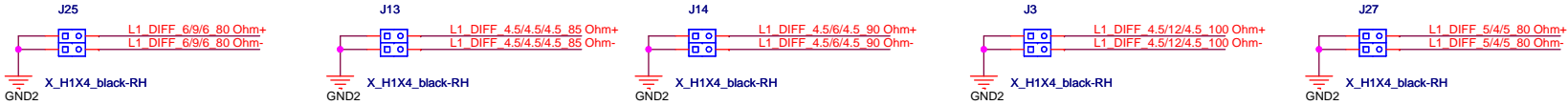


BOTTOM

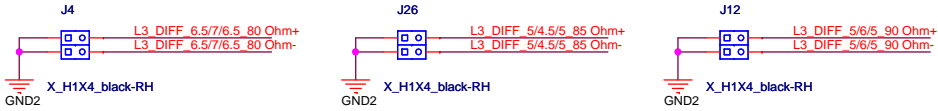


Differential signal

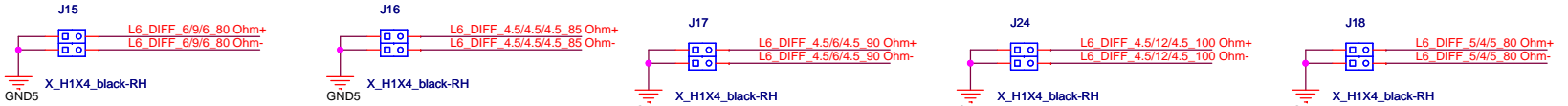
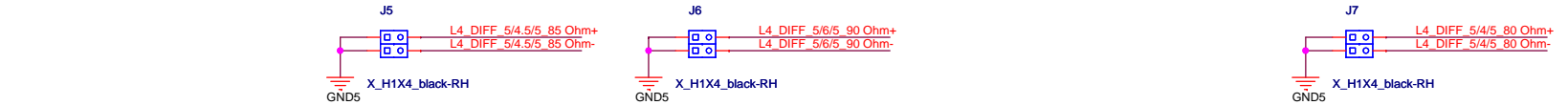
TOP



IN3

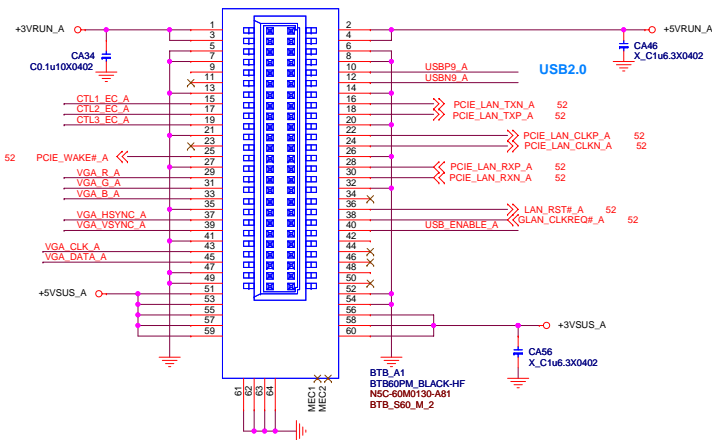


IN4

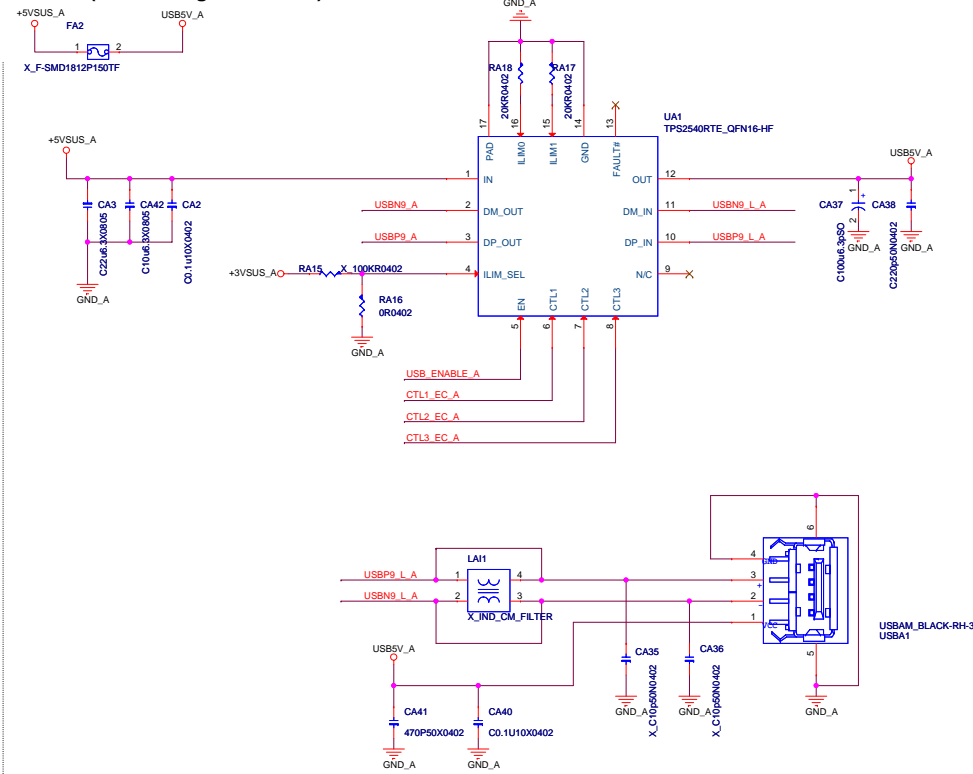


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Date:	Tuesday, December 03, 2013		Sheet 50 of 59

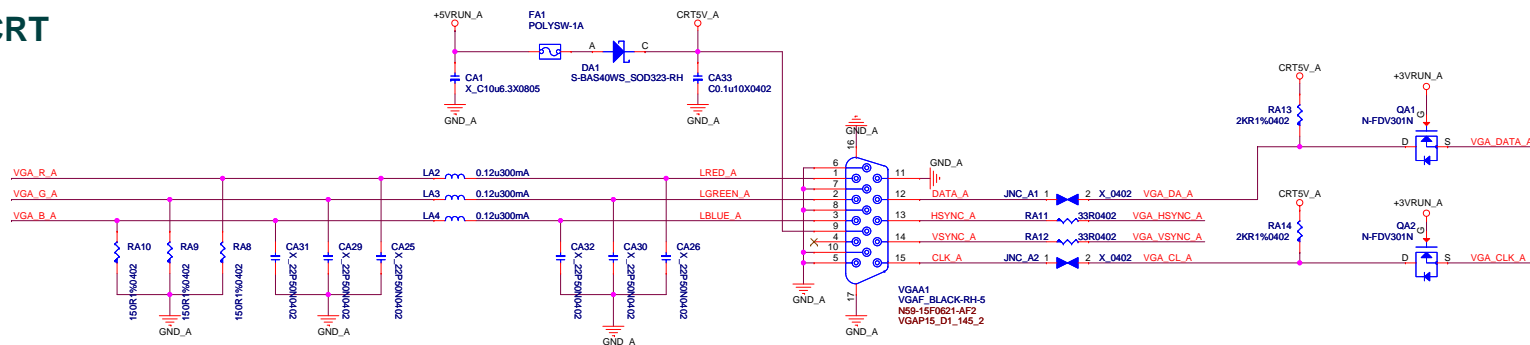
60PIN BTB I/O Connector(VGA, LAN, USB)



USB2.0 (I-Pad Charger Function)

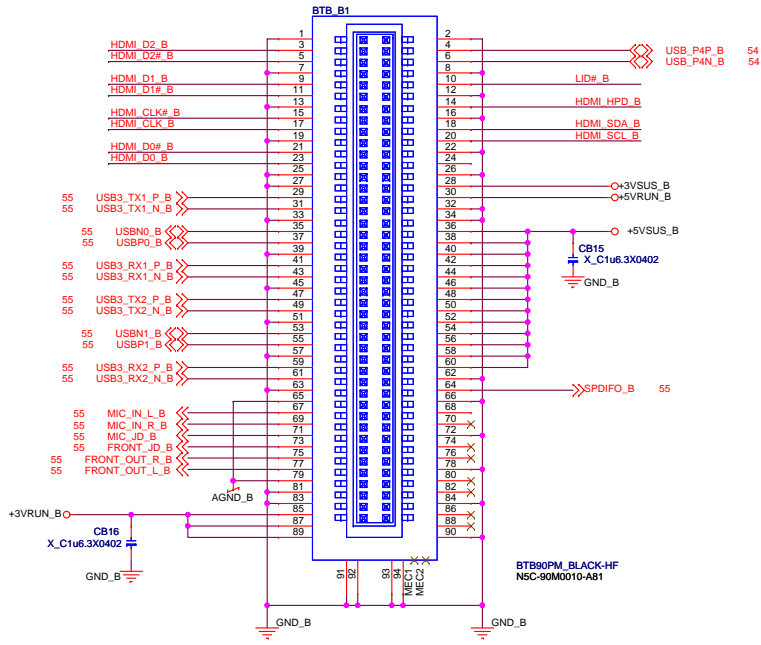


CRT

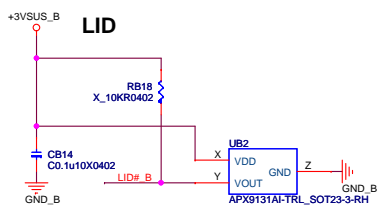


(才凹 board to board CONN1: HDMI,Audio, LED,LID)

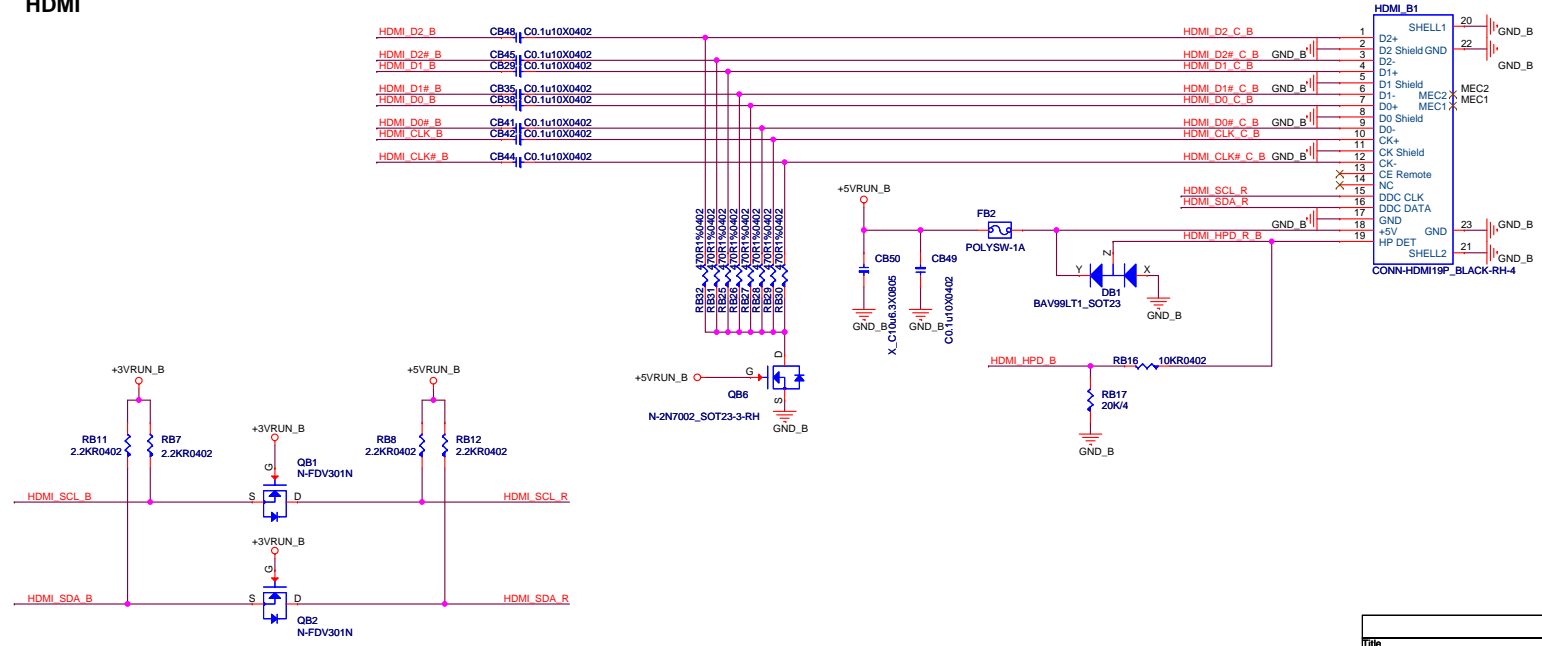
USB2.0 NC For 16GC



Hall Switch

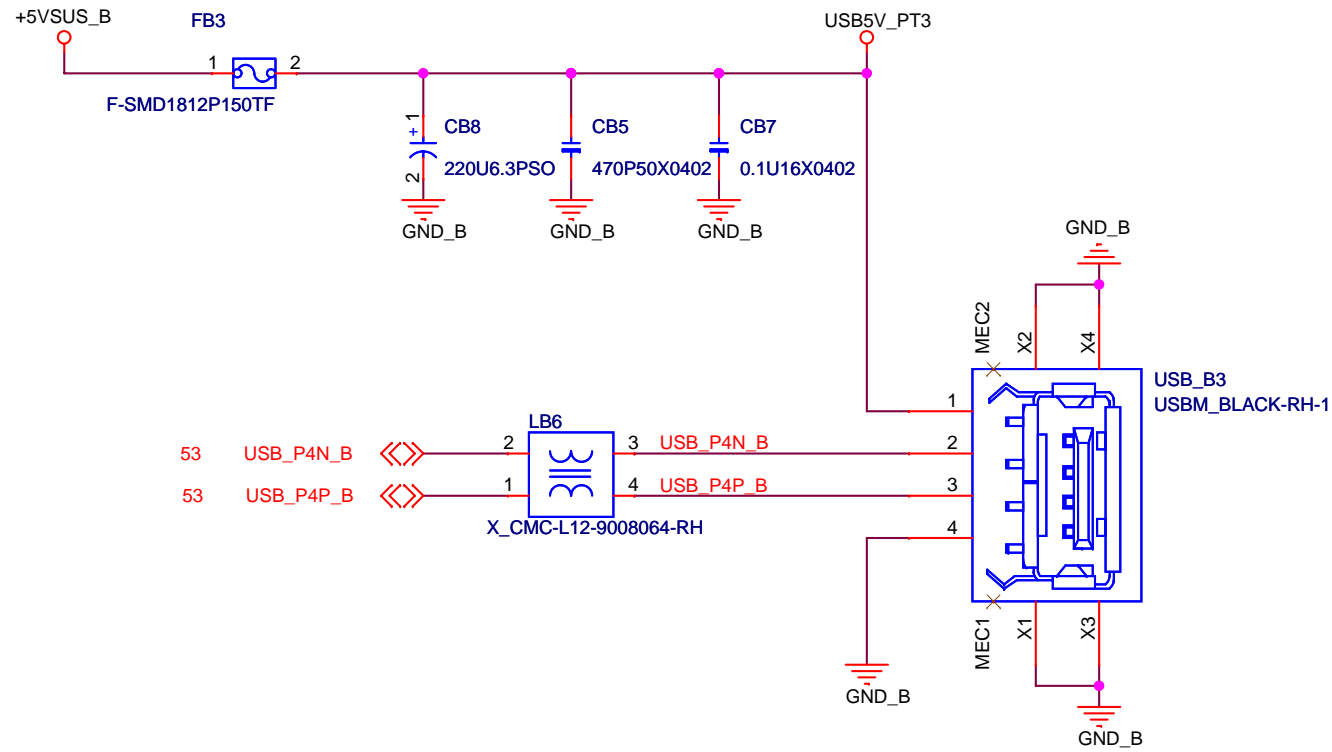


HDMI



Title			NP 5G5 6BAA"" : 7 <
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Date:	Tuesday, December 03, 2013	Sheet	53 of 59

USB2.0



Title		
N5P HF5%#		
Size	Document Number	
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Date:	Tuesday, December 03, 2013	Sheet 54 of 59

USB 3.0 CNT1

fiHF5'?XgFVW
z'HCf1

USB5V_PT1
USB5V_PT2
FB1
F-SMD1812P150TF
C843
C23050N0402
GND_B
C827
X_470P50X0402
GND_B
C826
C0.1u10X0402
GND_B
C828
220uE3P50
GND_B
C823
C10u6.3X0805
+5VSUS_B

USB5V_PT2
GND_B
VBUS
SSTX+
SSTX-
GND
SSRX+
SSRX-
GND
USB_B2
USB30_CON
GND_B

USBNO_B C
USBPO_B C
GND_B
SSTX1P_C_B
SSTX1N_C_B
GND
USB3_TX1_P_B
USB3_TX1_N_B
GND
USB3_RX1_P_B
USB3_RX1_N_B
GND

USB 3.0 CNT2

fiHF5'?XgFVW z'7bj afl

USB5V_PT1
GND_B
VBUS
SSTX+
SSTX-
GND
SSRX+
SSRX-
GND
USB_B1
USB30_CON
GND_B

USB1_B C
USBP1_B C
GND_B
SSTX2P_C_B
SSTX2N_C_B
GND
USB3_TX2_P_B
USB3_TX2_N_B
GND
USB3_RX2_P_B
USB3_RX2_N_B
GND

SCREW HOLE

BTB STANDOFF

Top side

HOLES_8X8_D3MM_VIA8
MH54
X_8x8
5
6
7
8
9
GND_B

HOLES_8X8_D3MM_VIA8
MH51
X_8x8
5
6
7
8
9
GND_B

HOLES236D118_P
MH53
X_HOLES236D118_P
5
6
7
8
9
GND_B

HOLES236D118_P
MH52
X_HOLES236D118_P
5
6
7
8
9
GND_B

MYLAR2
MYLAR_AUDIO_JACK
E2P-7214611-G40
Audio Jack Mylar
for EMI

UMEB2
ME
E2Y-2460111-Y42

UMEB1
X_ME
E2P-6G15011-Y42

PCB81
HDMI
ROYALTY

PCB_V08

Audio Jack

[Fuqun] ME change WLAN connect P/N from N54-06F1021-K06 to N54-06F1191-H06

MIC_IN_R_B
MIC_IN_L_B
MIC_ID_B
MIC_B1
JACK-AUDIOF_BL-SP-RH-5
(BLACK)
MIC Jack

SPDIF_B
LOUTJB_1A
JACK_SPDIF-RH-8
SPDIF_MINI_JACK
NS8-10F0071-H06

[Fuqun] ME change WLAN connect P/N from N58-10F0061-K06 to N58-10F0071-H06

FRONT_OUT_L_B
FRONT_OUT_R_B
FRONT_OUT_LL_B
FRONT_OUT_RL_B
FRONT_ID_B
JACK_SPDIF-RH-8
SPDIF_MINI_JACK
NS8-10F0071-H06

Power

QB27 VGS_ON : -1V~-2V

FRONT_ID=1.89V

FRONT_ID_B

ME HE5' 4hWb

Size 1 Document Number

Custom

@F7' 5

Date: Tuesday, December 03, 2013

Sheet 55 of 59

Rev 11

[illegible][illegible][illegible]

USB 3.0 CNT1

fiHF5'?XgFVW
z'HCf1

USB5V_PT1
USB5V_PT2
FB1
F-SMD1812P150TF
C843
C827
C826
C828
C22050N0402
X_470P50X0402
C0.1u10X0402
GND_B
220uE3P50
C823
C10u6.3X0805
+5VSUS_B

USB5V_PT2
GND_B
VBUS
SSTX+
SSTX-
D-
SSRX+
SSRX-
GND
USB_B2
USB30_CON
GND_B

USBNO_B C
USBP0_B C
GND_B
SSTX1P C_B
SSTX1N C_B
USB3_TX1_P_B
USB3_TX1_N_B
USB3_RX1_P_B
USB3_RX1_N_B

USB 3.0 CNT2

fiHF5'?XgFVW z'7bj afl

USB5V_PT1
GND_B
VBUS
SSTX+
SSTX-
D-
SSRX+
SSRX-
GND
USB_B1
USB30_CON
GND_B

USB1_B C
USBP1_B C
GND_B
SSTX2P C_B
SSTX2N C_B
USB3_TX2_P_B
USB3_TX2_N_B
USB3_RX2_P_B
USB3_RX2_N_B

SCREW HOLE

BTB STANDOFF

Top side

HOLES_8X8_D3MM_VIA8
MH54
X_8u8
5
6
7
8
9
GND_B

HOLES_8X8_D3MM_VIA8
MH51
X_8u8
5
6
7
8
9
GND_B

HOLES236D118_P
MH53
X_HOLES236D118_P
GND_B

HOLES236D118_P
MH52
X_HOLES236D118_P
GND_B

MYLAR2
MYLAR_AUDIO_JACK
E2P-7214611-G40
Audio Jack Mylar
for EMI

UMEB2
ME
E2Y-2460111-Y42

UMEB1
X_ME
E2P-6G15011-Y42

PCB81
HDMI
ROYALTY

PCB_V08

Audio Jack

[Fuqun] ME change WLAN connect P/N from N54-06F1021-K06 to N54-06F1191-H06

MIC_IN_R_B
MIC_IN_L_B
MIC_ID_B
MIC_B1
JACK-AUDIOF_BL-SP-RH-5
(BLACK)
MIC Jack

SPDIF_B
LOUTJB_1A
JACK_SPDIF-RH-8
SPDIF_MINI_JACK
NS8-10F0071-H06

[Fuqun] ME change WLAN connect P/N from N58-10F0061-K06 to N58-10F0071-H06

FRONT_OUT_L_B
FRONT_OUT_R_B
FRONT_OUT_LL_B
FRONT_OUT_RL_B
FRONT_ID_B
JACK_SPDIF-RH-8
SPDIF_MINI_JACK
NS8-10F0071-H06

Power

QB27 VGS_ON : -1V~-2V

FRONT_ID=1.89V

FRONT_ID_B

ME HE5' 4hWb

Size 1 Document Number

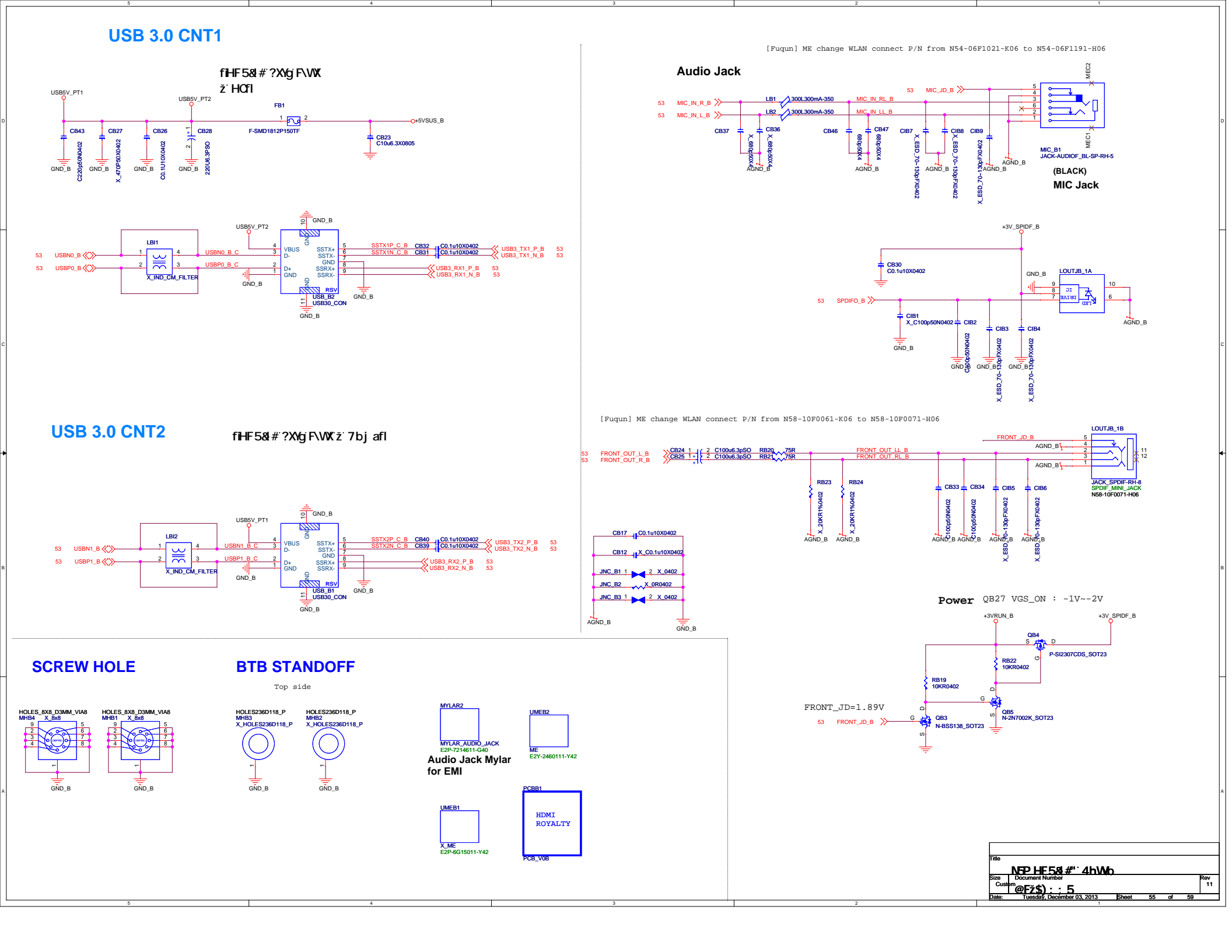
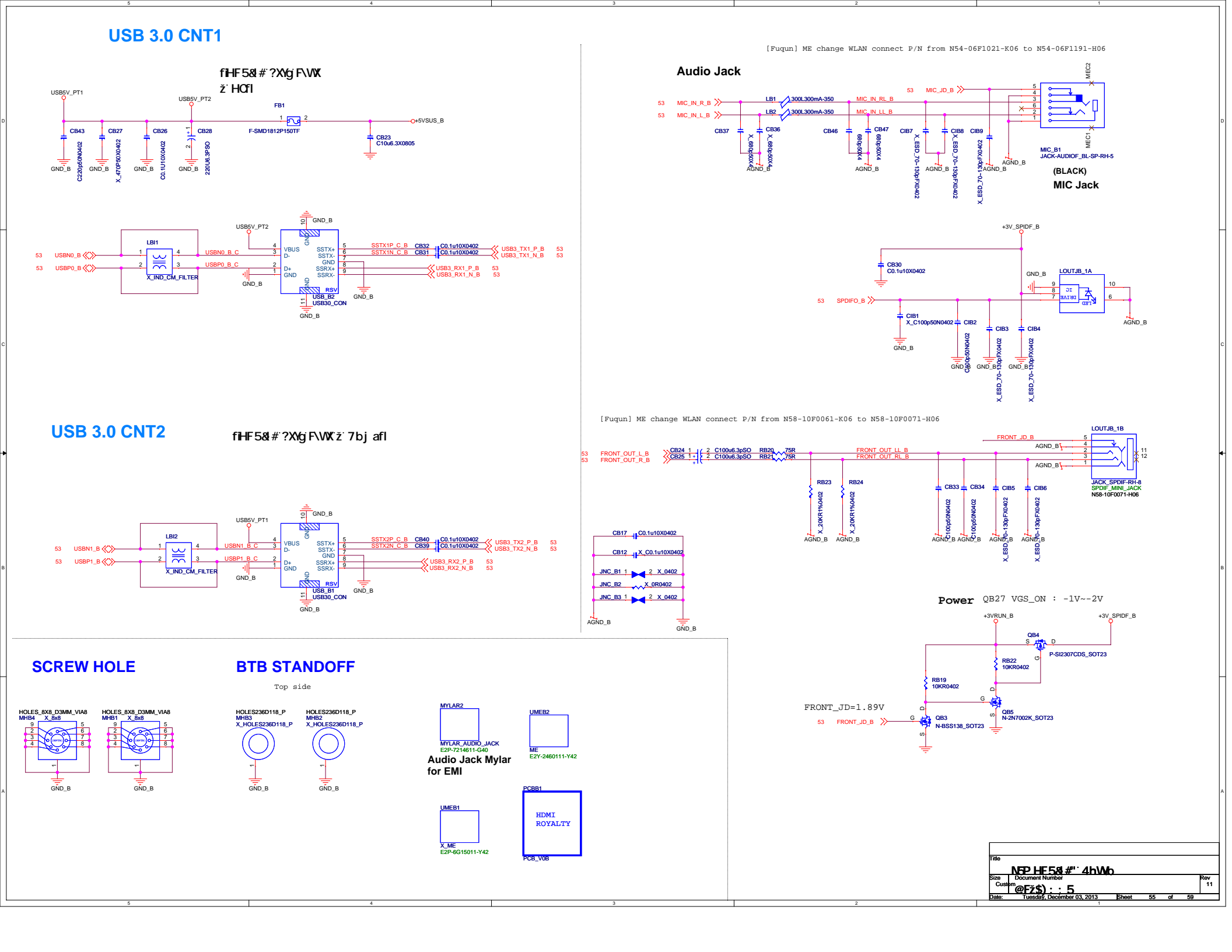
Custom

@F7' 5

Date: Tuesday, December 03, 2013

Sheet 55 of 59

Rev 11

[illegible]

USB 3.0 CNT1

fiHF5'?XgFVW
z'HCf1

USB5V_PT1
USB5V_PT2
FB1
F-SMD1812P150TF
C843
C23050N0402
GND_B
C827
X_470P50X0402
GND_B
C826
C0.1u10X0402
GND_B
C828
220uE3P50
GND_B
C823
C10u6.3X0805
+5VSUS_B

USB5V_PT2
GND_B
VBUS
SSTX+
SSTX-
D-
GND
SSRX+
SSRX-
GND
USB_B2
USB30_CON
GND_B

USBNO_B C
USBP0_B C
GND_B
SSTX1P_C_B
SSTX1N_C_B
USB3_TX1_P_B
USB3_TX1_N_B
USB3_RX1_P_B
USB3_RX1_N_B

USB 3.0 CNT2

fiHF5'?XgFVW z'7bj afl

USB5V_PT1
GND_B
VBUS
SSTX+
SSTX-
D-
GND
SSRX+
SSRX-
GND
USB_B1
USB30_CON
GND_B

USB1_B C
USBP1_B C
GND_B
SSTX2P_C_B
SSTX2N_C_B
USB3_TX2_P_B
USB3_TX2_N_B
USB3_RX2_P_B
USB3_RX2_N_B

SCREW HOLE

BTB STANDOFF

Top side

HOLES_8X8_D3MM_VIA8
MH54
X_8x8
5
6
7
8
9
GND_B

HOLES_8X8_D3MM_VIA8
MH51
X_8x8
5
6
7
8
9
GND_B

HOLES236D118_P
MH53
X_HOLES236D118_P
5
6
7
8
9
GND_B

HOLES236D118_P
MH52
X_HOLES236D118_P
5
6
7
8
9
GND_B

MYLAR2
MYLAR_AUDIO_JACK
E2P-7214611-G40
Audio Jack Mylar
for EMI

UMEB2
ME
E2Y-2460111-Y42

UMEB1
X_ME
E2P-6G15011-Y42

PCB81
HDMI
ROYALTY

PCB_V08

Audio Jack

[Fuqun] ME change WLAN connect P/N from N54-06F1021-K06 to N54-06F1191-H06

MIC_IN_R_B
MIC_IN_L_B
MIC_ID_B
MIC_B1
JACK-AUDIOF_BL-SP-RH-5
(BLACK)
MIC Jack

SPDIF_B
LOUTJB_1A
JACK_SPDIF-RH-8
SPDIF_MINI_JACK
NS8-10F0071-H06

[Fuqun] ME change WLAN connect P/N from N58-10F0061-K06 to N58-10F0071-H06

FRONT_OUT_L_B
FRONT_OUT_R_B
FRONT_OUT_LL_B
FRONT_OUT_RL_B
FRONT_ID_B
JACK_SPDIF-RH-8
SPDIF_MINI_JACK
NS8-10F0071-H06

Power

QB27 VGS_ON : -1V~-2V

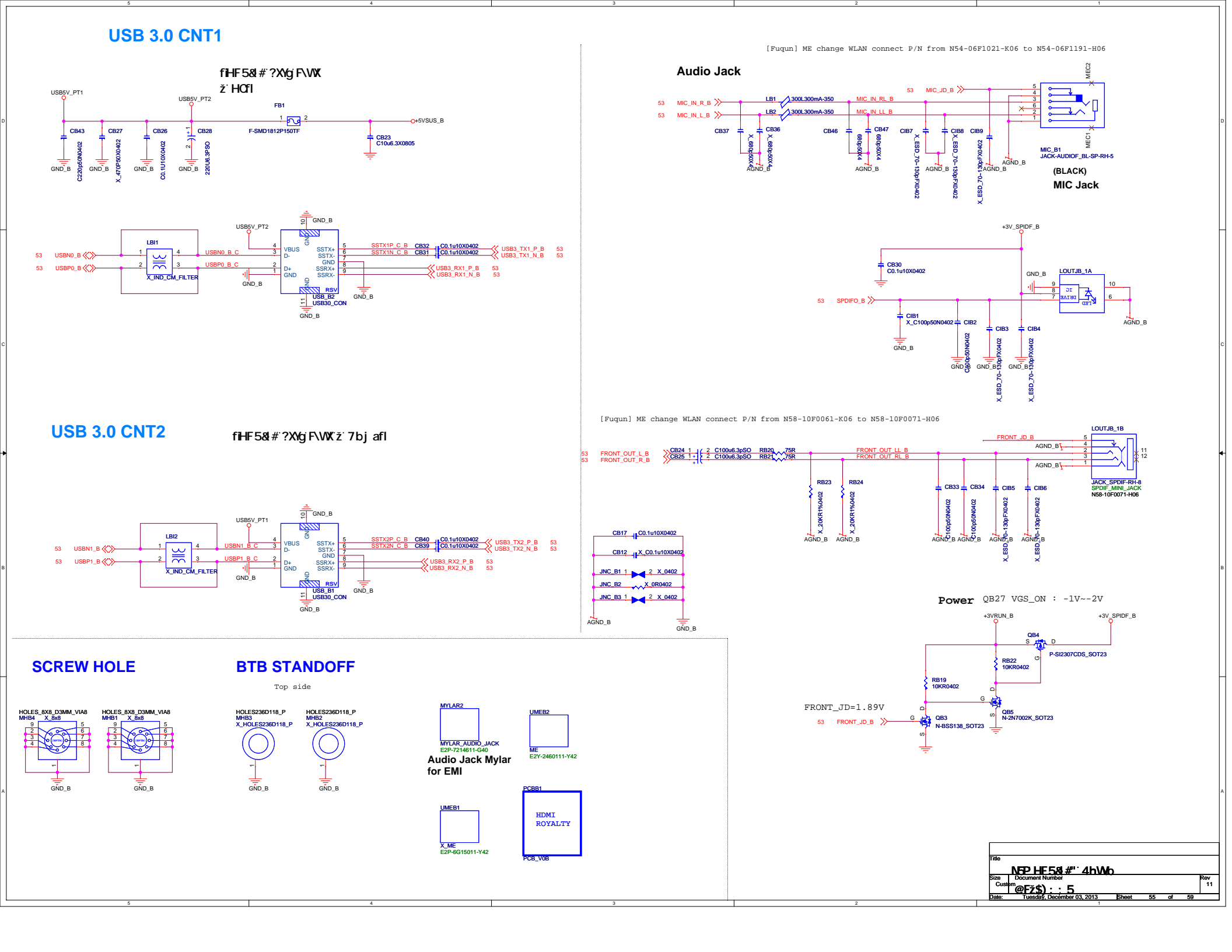
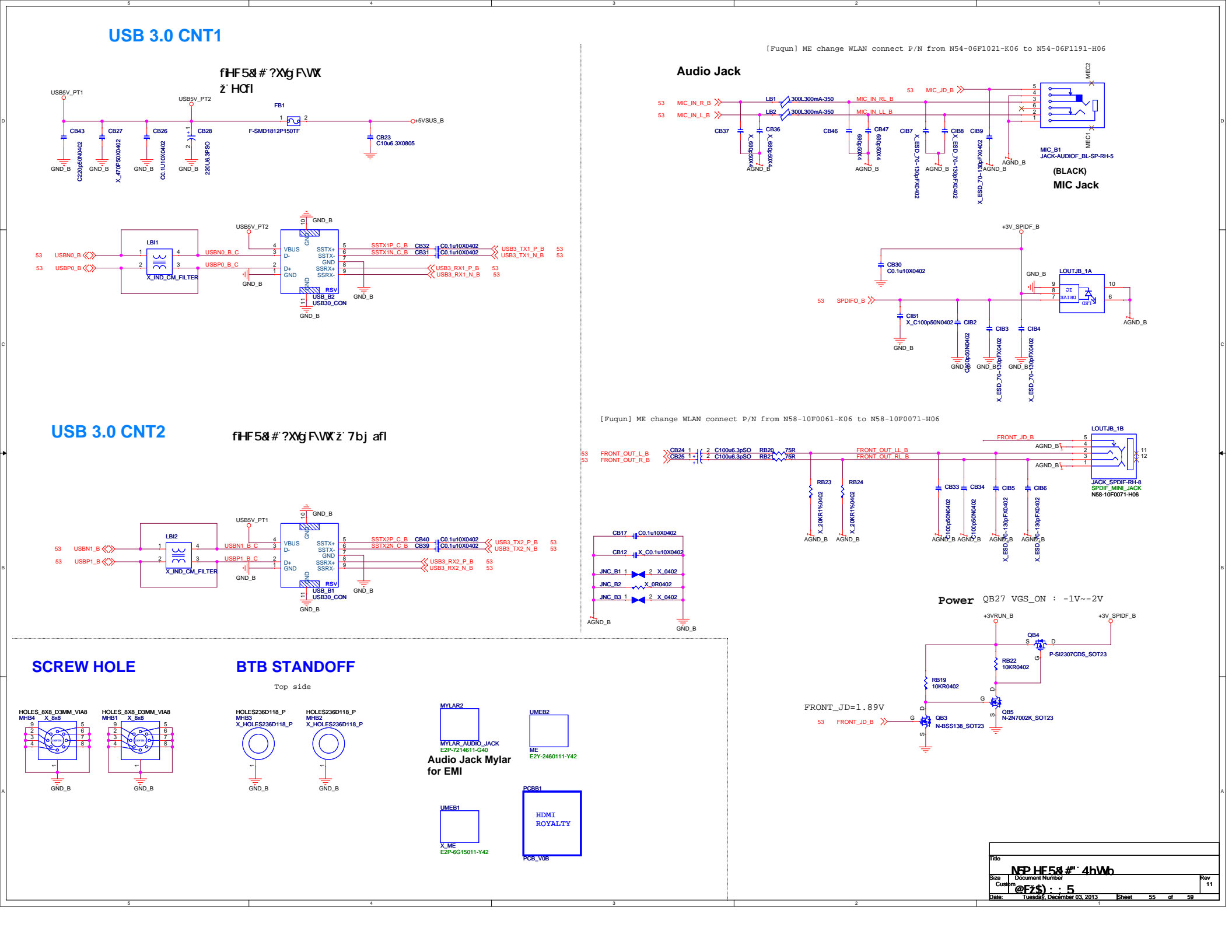
FRONT_ID=1.89V

FRONT_ID_B

ME HE5' 4hWb

Size 1 Document Number
Custom
@F7' 5

Date: Tuesday, December 03, 2013 Sheet 55 of 59

[illegible][illegible]

USB 3.0 CNT1

fiHF5'?XgFVW
z'HCf1

USB5V_PT1
USB5V_PT2
FB1
F-SMD1812P150TF
C843
C23050N0402
GND_B
C827
X_470P50X0402
GND_B
C826
C0.1u10X0402
GND_B
C828
220uE3P50
GND_B
C823
C10u6.3X0805
+5VSUS_B

USB5V_PT2
GND_B
VBUS
SSTX+
SSTX-
GND
SSRX+
SSRX-
GND
USB_B2
USB30_CON
GND_B

USBNO_B C
USBP0_B C
GND_B
SSTX1P_C_B
SSTX1N_C_B
GND
USB3_TX1_P_B
USB3_TX1_N_B
GND
USB3_RX1_P_B
USB3_RX1_N_B
GND

USB 3.0 CNT2

fiHF5'?XgFVW z'7bj afl

USB5V_PT1
GND_B
VBUS
SSTX+
SSTX-
GND
SSRX+
SSRX-
GND
USB_B1
USB30_CON
GND_B

USB1_B C
USBP1_B C
GND_B
SSTX2P_C_B
SSTX2N_C_B
GND
USB3_TX2_P_B
USB3_TX2_N_B
GND
USB3_RX2_P_B
USB3_RX2_N_B
GND

SCREW HOLE

BTB STANDOFF

Top side

HOLES_8X8_D3MM_VIA8
MH54
X_8x8
5
6
7
8
9
GND_B

HOLES_8X8_D3MM_VIA8
MH51
X_8x8
5
6
7
8
9
GND_B

HOLES236D118_P
MH53
X_HOLES236D118_P
5
6
7
8
9
GND_B

HOLES236D118_P
MH52
X_HOLES236D118_P
5
6
7
8
9
GND_B

MYLAR2
MYLAR_AUDIO_JACK
E2P-7214611-G40
Audio Jack Mylar
for EMI

UMEB2
ME
E2Y-2460111-Y42

UMEB1
X_ME
E2P-6G15011-Y42

PCB81
HDMI
ROYALTY

PCB_V08

Audio Jack

[Fuqun] ME change WLAN connect P/N from N54-06F1021-K06 to N54-06F1191-H06

MIC_IN_R_B
MIC_IN_L_B
MIC_ID_B
MIC_B1
JACK-AUDIOF_BL-SP-RH-5
(BLACK)
MIC Jack

SPDIF_B
LOUTJB_1A
JACK_SPDIF-RH-8
SPDIF_MINI_JACK
NS8-10F0071-H06

[Fuqun] ME change WLAN connect P/N from N58-10F0061-K06 to N58-10F0071-H06

FRONT_OUT_L_B
FRONT_OUT_R_B
FRONT_OUT_LL_B
FRONT_OUT_RL_B
FRONT_ID_B
JACK_SPDIF-RH-8
SPDIF_MINI_JACK
NS8-10F0071-H06

Power

QB27 VGS_ON : -1V~-2V

FRONT_ID=1.89V

FRONT_ID_B

ME HE5' 4hWb

Size 1 Document Number

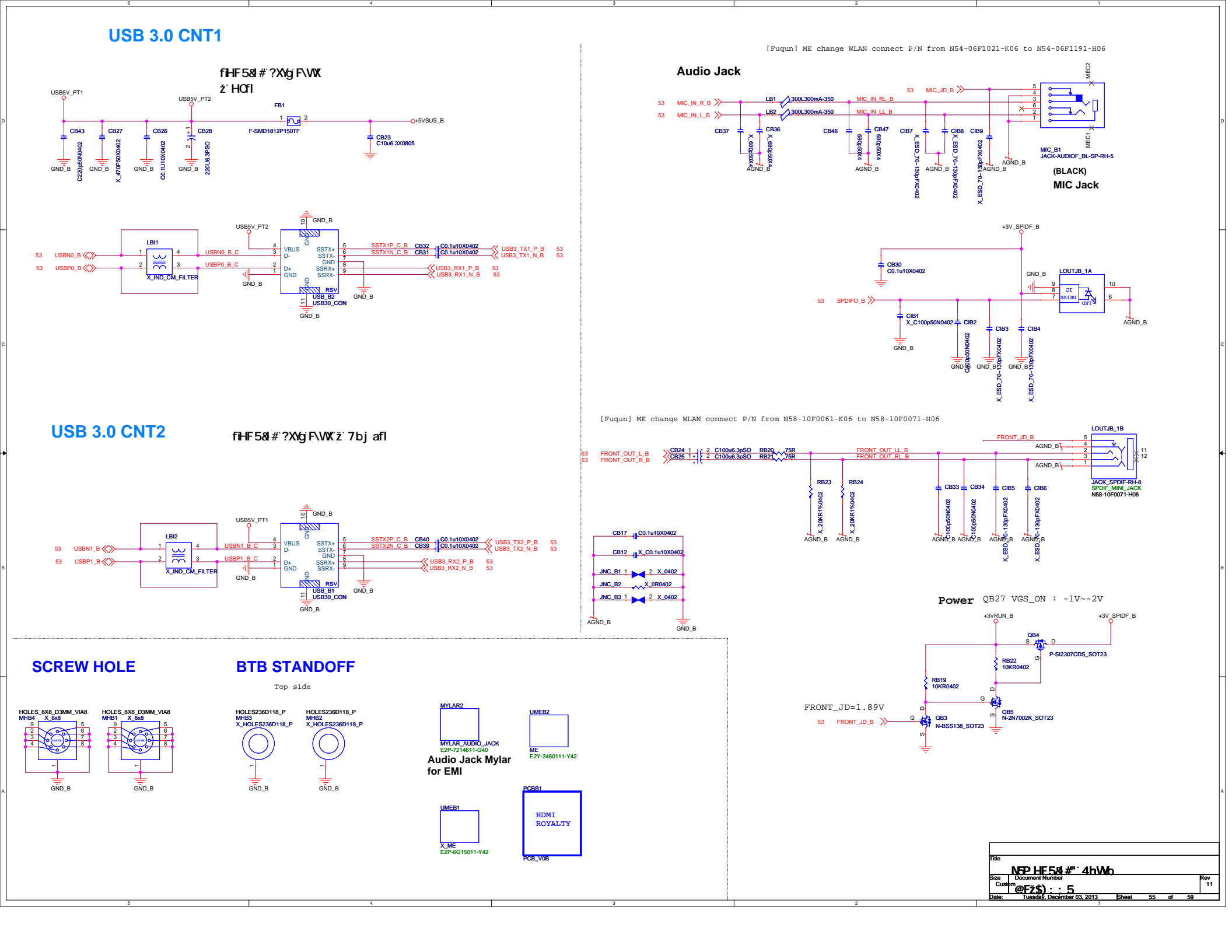
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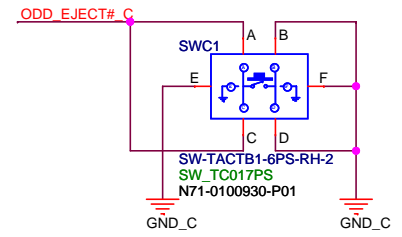
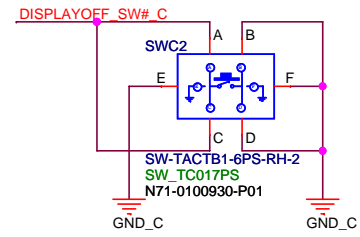
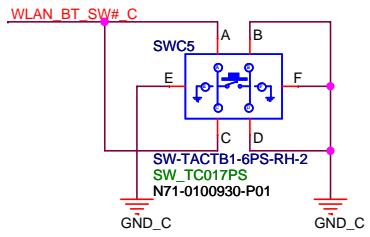
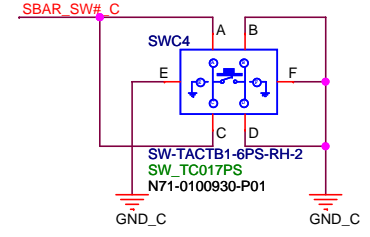
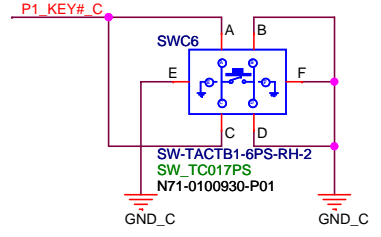
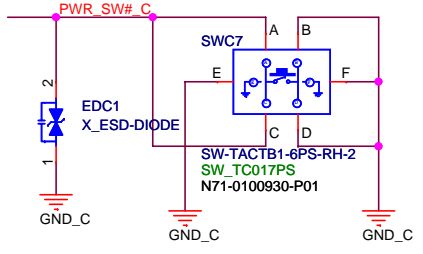
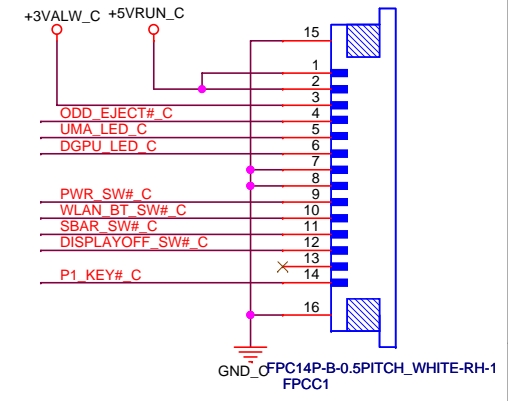
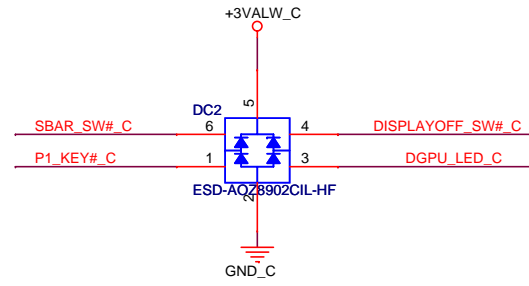
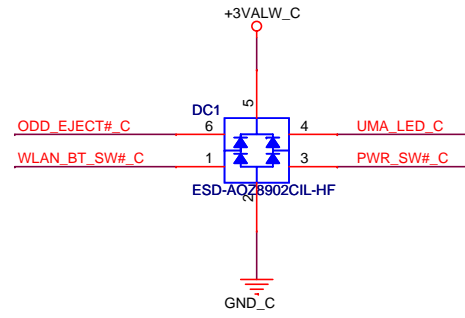
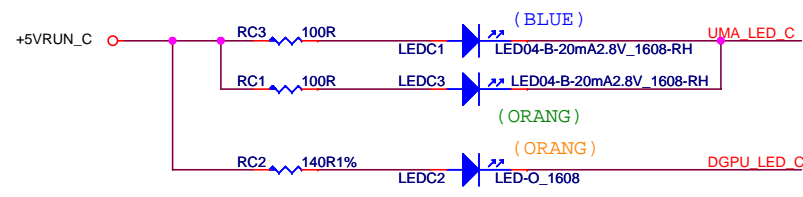
@F7' 5

Date: Tuesday, December 03, 2013

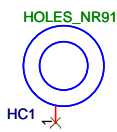
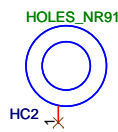
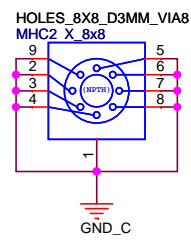
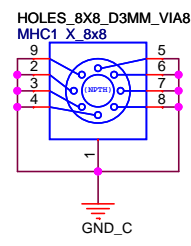
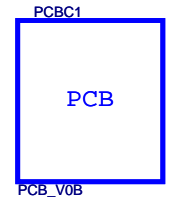
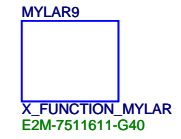
Sheet 55 of 59

Rev 11

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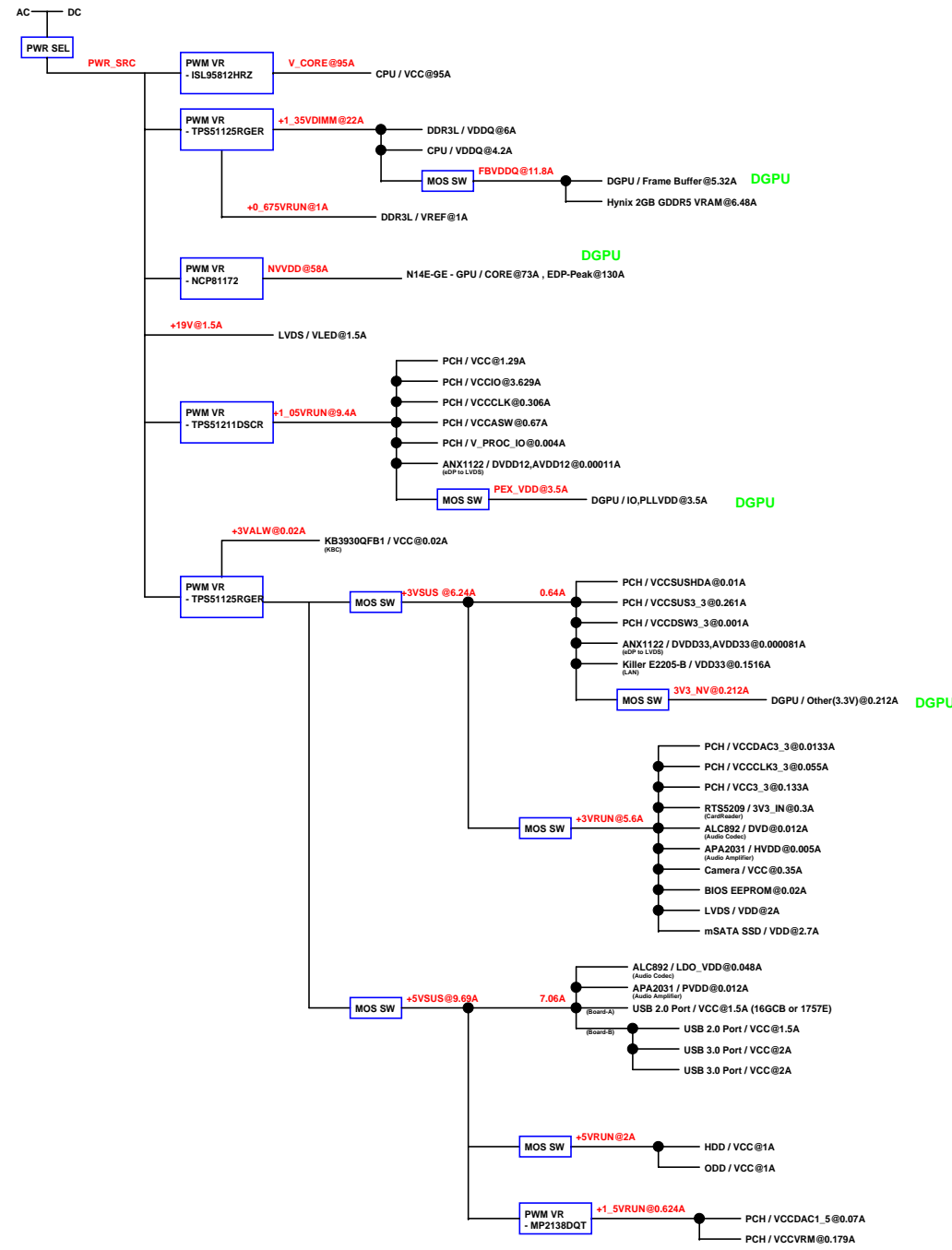


[Fuqun] EMI remove E2M-7511611-G40

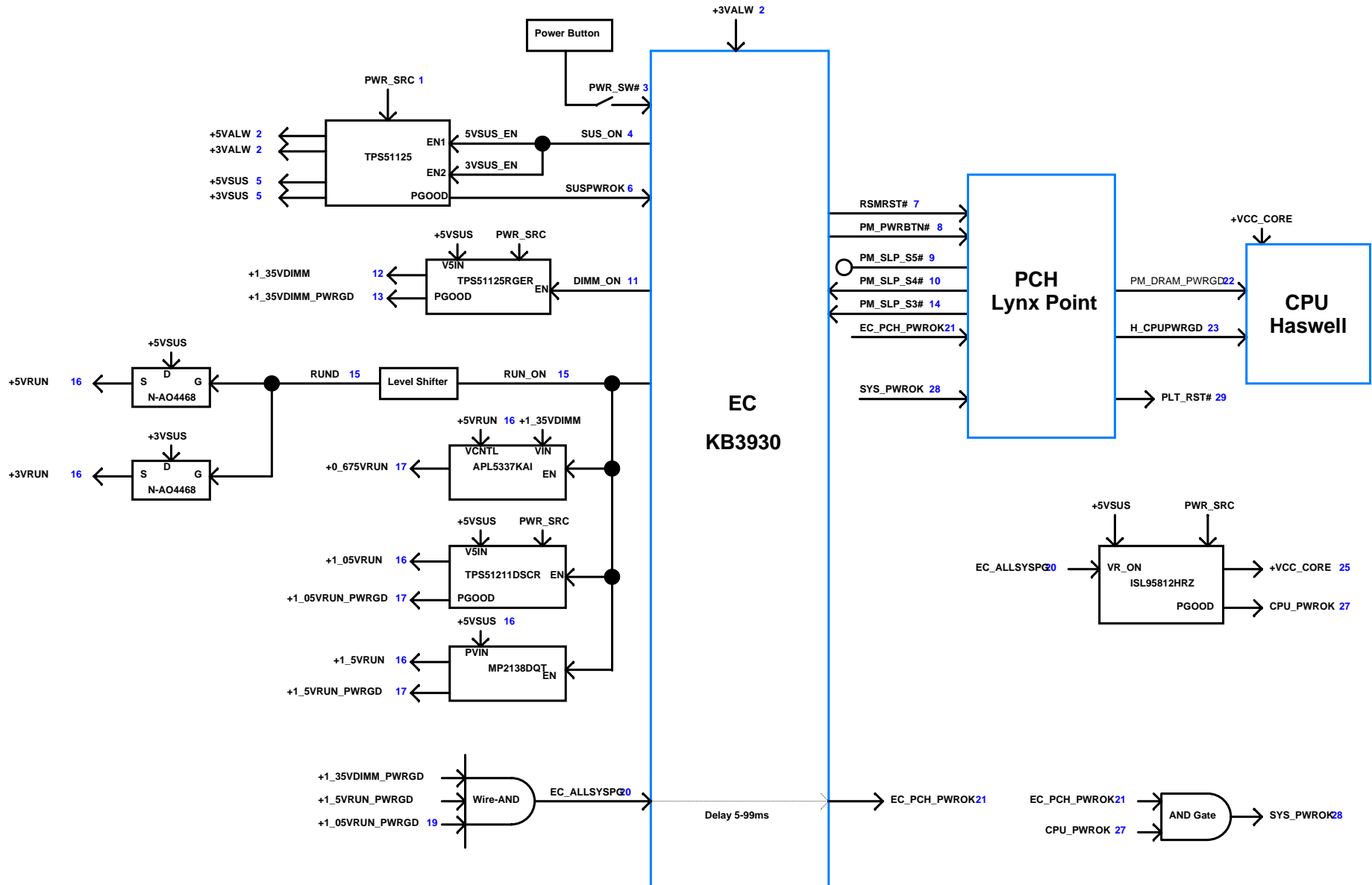


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N6P Cbj XeF J 5bTeW		
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Custom	@F7\$): : 6	11
Date:	Tuesday, December 03, 2013	Sheet 56 of 59

1757 Power Delivery Chart



1757 Power on Block Diagram



Power on Sequence

G3 -> S0

